(12) EUROPEAN PATENT APPLICATION

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(54) Method and system for a multi channel and search global position signal processor.

(57) There is disclosed a multi channel GPS digital signal processor on a single IC. Each channel (11,12) contains circuitry to process L1 or L2 P(Y) and C/A-code signals. In addition a search processor (123) is included to achieve fast signal acquisition. Low power adder/accumulators (3901-Fig.4) have been designed to provide for a high precision digital oscillator (103 ; 104) whose output is synchronous to a high speed clock. The IC contains a full low power null detector and eight correlators (111, 113, 115, 117 ; 112, 114, 116, 118).

FIG. 1
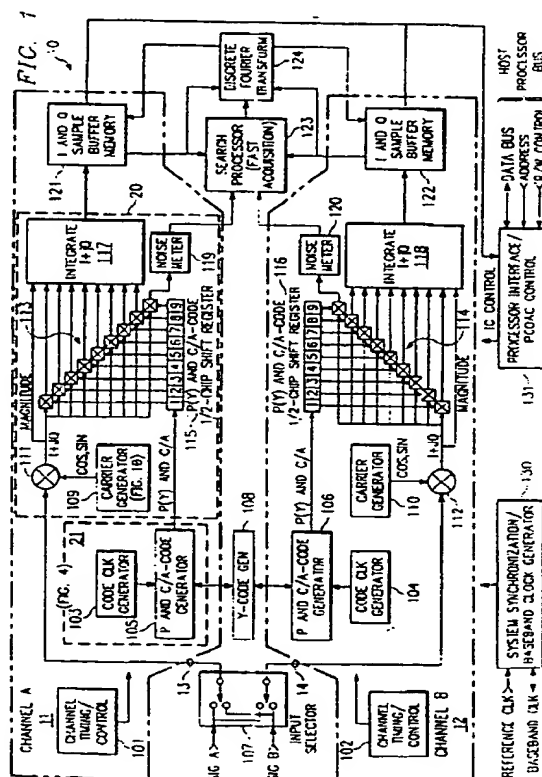
EP 0 501 828 A1

TECHNICAL FIELD OF THE INVENTION

This invention relates to global positioning signalling and more particularly to a device for achieving multi channel and search processing for a global position system.

BACKGROUND OF THE INVENTION

The Navstar Global positioning System (GPS) is used to determine exact geographic position (i.e., latitude, longitude and altitude) absolute velocity as well as the exact time. The navigation device must calculate the position, velocity and the time by determining distance and relative velocity to a series of satellites. The velocity of the receiver is calculated from the doppler frequency shift of signals transmitted from the satellites. This distance is called range and the doppler shift yields range rate.

A GPS receiver must receive signals generated from a satellite about 11,000 miles away. A GPS satellite transmits about a 6 watt spread spectrum signal. The satellite and receiver, therefore, has to employ spread spectrum techniques to differentiate the signal from the noise. "Spread spectrum" means that the frequency or instantaneous phase of the signal being transmitted changes as a function of time. Using correlation techniques, the receiver can track the spread spectrum signal coming from the satellite by estimating a duplicate image of the signal. A precise match of the satellite's spread spectrum produces a potential signal processing gain of up to 53 decibels. The use of spread spectrum techniques is essential to receive 6 watts of energy transmitted 11,000 miles away. At the antenna, the GPS signal is about 20 dB below ambient cosmic noise.

Prior GPS digital receivers performed signal processing functions in the analog domain thereby requiring many expensive discrete components, some of which needed to be tuned to match the circuitry. A common cost/performance tradeoff was to multiplex or sequence one or two channels.

By digitizing the GPS signal at the final IF stage and performing all channel signal processing functions digitally in a low cost CMOS IC, GPS receiver performance is greatly improved and cost is reduced. Such a system is disclosed in concurrently filed copending patent application entitled "System and Method for a Digital Navigation Satellite Receiver," which patent is hereby incorporated by reference herein.

While the IC presents significant benefit to a GPS receiver, it also presents several problems in building an IC that is low cost and consumes little power. Digitizing the GPS signal at the final IF requires high frequency operation for a signal processing device, i.e. 40 to 60 megahertz for a double sideband GPS signal. Features in a GPS signal processing device which improve performance in hostile environments include full null zone signal integration, multiple correlators, anti-spoofing, and a search processor for fast acquisition.

When all these features are combined in one chip, it is very difficult to meet power consumption goals for the device and to minimize the gate count of the device, thereby minimizing its cost. In addition to the cost of the IC, there is a finite limit to the number of gates which can be put on the IC and thus designing a circuit that will fit on a single IC is difficult.

SUMMARY OF THE INVENTION

We successfully integrated all the aforementioned high performance features into a single IC containing two complete GPS signal processing channels and a search processor for fast acquisition.

In order to meet these high performance requirements, we designed a special adder/accumulator architecture for high speed sample integration compatible with full null zone anti-jamming techniques. A similar architecture also reduces gate count in the carrier and code block digital oscillators.

We also designed an architecture for correlators which greatly reduces power and gate count. This architecture also supports full null zone and a feature called "adjacent correlator presumming".

Lastly we implemented a digital oscillator architecture which, while running synchronous to the high frequency between 40 and 60 megahertz, the majority of the circuitry runs at one-eighth of that frequency, thereby reducing power.

Accordingly, one technical advantage of our invention is that there is provided an adder/accumulator which supports full null zone and greatly reduces power.

It is further technical advantage of our invention that a GPS receiver circuit uses a low gate count adder/accumulator for providing a digital oscillator.

It is a further technical advantage of our invention to provide a low power high precision digital oscillator whose output is synchronous to a high speed clock.

It is a further technical advantage of our invention that a complete automonous search processor which implements an 8-point DFT and Tong detection algorithm is included which can control either or both channels during search operations.

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It is a further technical advantage of our invention that there are two channels included, each of which can track L1 or L2 or Y-code and C/A-code simultaneously and that the Y-code generation function is included in the IC.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention may be acquired by referring to the detailed description and claims considered in connection with the accompanying drawings in which like reference numbers indicate like features wherein:

FIGURES 1 and 2 show block diagrams of the system;
FIGURE 3 shows the prior art of a conventional adder/accumulator digital oscillator;
FIGURE 4 shows the approach taken for the code clock generator;
FIGURES 5, 6 and 7 show state diagrams for the code clock generator;
FIGURE 8 shows state machine operation versus frequency plan;
FIGURE 8A shows the three most significant bits of the phase word as a function of S;
FIGURE 9 highlights the operational performance of the code clock generator;
FIGURE 10 shows a block diagram of the carrier generator;
FIGURE 11 shows the carrier generator state diagram;
FIGURE 12 highlights operational performance of the carrier generator;
FIGURE 13 shows frequency dependent phase bias;
FIGURE 14 lists the thirty largest phase settability anomalies;
FIGURES 15, 16 and 17 show the phase settability anomalies for the code clock generator;
FIGURES 18 and 19 show the phase range of each state for the code clock generator;
FIGURES 20 shows the same for the carrier generator;
FIGURE 21 shows the non-orthogonal axes for the carrier generator;
FIGURES 22 shows the phase settability anomalies for the carrier generator;
FIGURE 23 shows prior art for a 6-bit adder/accumulator;
FIGURE 24 shows a block diagram of the special adder/accumulator;
FIGURES 25-28 show how a special adder/accumulator is built;
FIGURE 29 shows a block diagram of the intermediate correlator module;
FIGURES 30 and 31 show the pulse generators required for the special adder/accumulator;
FIGURES 32-35 discuss valid inputs for this adder/accumulator;
FIGURE 36 shows a special cell which was generated to achieve a balanced rise and fall time;
FIGURE 37 shows the special adder/accumulator cell;
FIGURE 38 shows a 4-bit adder/accumulator with carry;
FIGURES 39a and 39b show the adder/accumulator with latches;
FIGURE 40 shows a block diagram of the back-end correlator module;
FIGURE 41 shows how the eight complex adder/accumulators are built;
FIGURE 42 shows how the pulse encoder works;
FIGURE 43 shows a detailed circuit of the sample accumulators;
FIGURE 44 describes adjacent correlator presumming;
FIGURE 45 shows performance without adjacent correlator presumming; and
FIGURE 46 shows performance with adjacent correlator presumming.

DETAILED DESCRIPTION OF THE INVENTION

The P-Code Channel on-a-Chip (PCOAC) of the instant invention is a dual channel GPS signal processor integrated circuit. A 95-pin ceramic pin-grid-array (PGA) contains the 348,300 transistor CMOS gate array. Major features include: two independent GPS channels; a search processor for improved acquisition time; an embedded Y-code generator: system synchronization control; and a 16-bit processor interface.

FIGURE 1 shows a block diagram of PCOAC 10. Unused functions can be turned off allowing for a high level of power conservation in applications where power usage and/or heat dissipation is an important consideration.

Each channel of circuit 10 is a dedicated signal processing circuit which de-modulates the code and carrier of a GPS signal and performs pre-detection integration. Each channel contains a code clock generator 103 (104), a P and C/A-code generator 105 (106), an L1/L2 carrier generator 109 (110), eight correlators 111, 113, 115, 117 (112, 114, 116, 118) and a noise meter 119 (120). Each of the eight correlators can be selected to operate with C/A-code or P-code. A Y-code generator 108 common to both channels provides independent Y-

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code for both channels.

Search processor 123 and discrete fourier transform (DFT) function 124 improve signal acquisition capability. The DFT separates the sample integration data into seven frequency bins. Search processor 123 interpolates between these seven frequency bins to obtain six additional frequency bins, producing a total of thirteen frequency bins per correlator. The search processor implements a Tong detection algorithm on all eight correlators for each of the thirteen frequency bins resulting in the simultaneous search of 104 search bins per channel.

PCOAC 10 supports three frequency plans, 57.7920 MHz, 40.9216 MHz and 40.9200 MHz operation. Several programmable clocks/interrupts 130 are provided to synchronize the host processor to PCOAC operation. Various interrupt schemes are designed to allow trade-offs to be made between system performance, processor throughput requirements and the complexity of the software.

A standard 16-bits processor interface 131 is utilized. In order to minimize read/write overhead to the PCOAC, integration samples are buffered 121 (122) and the memory map is designed so that block moves are all that is required for channel updates during normal tracking operations.

FIGURE 2 is a block diagram of the top level modules which electrically make up channel A(11) of PCOAC 10;

Base Band Module 130 generates several global clocks for system synchronization:

Channel Timing Module 101 generates all clocks and synchronization pulses specific to a single channel;

Code generator Module 21 includes a programmable code clock generator, P-code and C/A-code generator/setters, and P-code and C/A-code state advance and retard for search;

Y-Code generator Module 108 converts the P-code into Y-code for both channels simultaneously even during code state advances;

Front-end Correlator Module 201 provides L1 or L2 carrier generation, a carrier mixer, a P-code and C/A-code delay shift register (to generate eight code phases), code mixers, data wipe-off, and noise meter signal selection;

Intermadiate Correlator Module 202 performs the first stage of sample integration for eight complex correlators and a noise meter;

Back-End Correlator Module 203 performs the final stage of sample integration, and also performs noise measurement for aiding in search and tracking (one per channel);

I RAM 204 and Q RAM 205 are two 64 x 16-bit 3-port RAMs per channel for sample integration buffering or to hold intermediate values for DFT calculations;

Discrete Fourier Transform (DFT) Module 124 converts integration samples from all correlators of both channels into seven frequency bins of sample data for search operations;

Search Processor Module 206 interpolates six additional frequency bins from those provided by the DFT module, performs Tong detection on all thirteen frequency bins of data and retards the code state until a signal is found;

Search Processor RAM 207 is a 64 x 16-bit 3-port RAM used by the search processor as a holding register for active Tong counts during search or noise measurement buffering during tracking;

Processor Interface Module 131 provides address decode to generate internal read and write strobes, integration sample buffering control, a programmable ring oscillator for test and other miscellaneous functions;

Digressing momentarily in order to receive spread spectrum signals, as in a GPS receiver, it is necessary to very closely match the signal generated by the signal source (i.e., the satellite). In GPS, two precisely controllable digital oscillators are required per channel, one to match the code frequency (nominally 10.23 MHz) and one to match the final carrier IF (between 10.1 and 15.1 MHz depending on receiver configuration). To meet nyquist sampling requirements, the PCOAC samples incoming signals at greater than 40 MHz (up to 57.792 MHz depending on which frequency plan is implemented in the receiver).

FIGURE 3 shows the most straightforward way (prior art) to implement a high precision digital oscillator, whose output is synchronous to a high speed clock. The circuit uses a loadable adder/accumulator 303, 304 & 305, pipelined as required. This approach was used in a single C/A-code channel or a chip previously developed.

Since this device sampled incoming signals at only 12.799 MHz, power was less of a consideration than gate count. However/ if on the PCOAC an adder/accumulator of adequate precision (32-bits) were to run a 57.792 MHz, it would consume about 150 mW of power. Since on the PCOAC, four such adder/accumulators are required (two per channel), total power consumed by these digital oscillators would be 600 mW.

Using an innovative low power approach, each digital oscillator in PCOAC 10 consumes only 43 mW on average at 57.792 MHz, saving a total of 428 mW par PCOAC or a total of 1.3 watts in a six channel receiver. Unlike the adder/accumulator digital oscillator approach, this approach limits the output frequency of the digital oscillator to a limited range about a center frequency. The more narrow that range is, the more power that can

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be conserved. Also, this approach requires slightly more gates than the conventional approach (roughly 5 to 30 percent more depending on the number of bits of precision and other design specifics).

As shown in FIGURES 4 and 10, this innovative approach is used in the PCOAC for code clock generator 103 (FIGURE 4) and carrier generator 109 (FIGURE 10). An approximation of a part of this approach is used for circuit simplification, causing some phase settability anomalies. Also, the carrier generator generates two 2-bit outputs 90° out of phase. These 2-bits outputs cause some additional phase settability anomalies.

Code clock generator 103 shown in FIGURE 4 is designed to generate a P-code clock with a nominal frequency of 10.2300 MHz. Phase and frequency of the P-code block is programmable via processor interface 131 (FIGURE 1) and bit latches 3904, 3905, 409.

FIGURE 9 shows the frequency range, frequency settability, and phase settability for the three reference clock frequencies of PCOAC 10.

The code clock output is generated by dividing down the reference clock by a programmable non-integer divisor. For example, in the 57.792 MHz plan, the reference clock is divided down by 5.649266862 to generate a code clock with a frequency of 10.23 MHz. To minimize power consumption, the code clock generator is designed to run a minimum of circuitry at reference clock frequency. Most of the code clock generator circuitry runs at one eighth the reference clock frequency. The benefit of low power is a tradeoff in performance in phase settability at certain frequencies.

State machine 408, which runs at the reference clock frequency, generates the final code clock output. Averaged over time, it divides the reference clock down by the desired divisor. On each reference clock active edge, the state machine advances the phase of the code clock by a fixed member of degrees. A carry input to the state machine modifies the number of degrees the code clock is advanced on a given reference clock active edge.

FIGURE 8 shows the number of degrees the code block phase is advanced on each reference clock and a result of each carry for each of the three frequency plans. This state machine is further illustrated in FIGURES 5, 6 & 7 for the 57.792 MHz plan, the 40.9216 MHz plan and the 40.9200 MHz plan, respectively. The phase advance assigned to each reference clock period and to each carry and the frequency of carries determines the average frequency of the code output.

Returning to FIGURE 4 (or FIGURE 10), 32-bit adder/accumulator 3901 determines the frequency of the carry input to the state machine. The 32-bit adder/accumulator is clocked once every eighth reference clock. Each time it is clocked, a frequency word provided by the host processor is added to the value held in the accumulator. Every time the accumulator rolls over, a carry signal is generated to the state machine. Therefore, the frequency of carries is calculated as follows:

$$(1) \qquad Fcarry = \frac{Fref}{8} \times \frac{FW}{2^{32}}$$

where Fcarry is the frequency of carries, Fref is the reference clock frequency and FW is the 32-bit frequency word provided by the host processor.

The average frequency of the code clock output is calculated as follows:

$$(2) \qquad Fcdclk = Fref \times \frac{PAref}{360} + Fcarry \times \frac{PAcarry}{360}$$

$$= Fref \times \frac{PAref}{360} + \frac{Fref}{8} \times \frac{FW}{2^{32}} \times \frac{PAcarry}{360}$$

$$= Fref \times \frac{(PAref + FW/2^{35} \times PAcarry)}{360}$$

where PAref is the phase advance per reference clock and PAcarry is the phase advance per carry (see FIG 8). Solving this equation for the frequency word (FW) yields the following equation.

$$(3) \qquad FW = \frac{2^{35}}{PAcarry} \left[360 \times \frac{Fcdclk}{Fref} - PAref \right]$$

$$= \left[Fcdclk - \left[\frac{Fref}{360} \times PAref \right] \right] \times \left[\frac{2^{35}}{PAcarry} \times \frac{360}{Fref} \right]$$

Carry delay circuit 407 improves instantaneous phase resolution and reduces frequency dependent phase bias. Each carry is delayed a number of reference clocks from the time the adder/accumulator rolls over depending on by how much the adder/accumulator overflows. Ideally, the carry should be delayed by:

$$(4) \quad Dcarry = INT (8 \times (1 - AW/FW))$$

where AW is the value of the word in the accumulator after it rolls over and Dcarry is the number of reference clocks to delay the carry. This approach causes a carry to occur eight reference clocks after when it would occur in a conventional adder/accumulator digital oscillator. This approach exactly matches the ideal performance of a digital oscillator with its adder/accumulator running at reference clock frequency, but uses less power because its adder/accumulator is running at one eighth the reference clock frequency.

Implementing the ideal carry delay described above would be difficult, therefore an approximation is implemented. The approximation implement delays the carry in accordance with the following equation:

$$(5) \quad Dcarry = 8 - INT (AW/2^{29})$$

where Dcarry is the number of reference clocks the carry is delayed. The reason this approximation is not exact for the full range of the frequency word is that the value left in the accumulator after a carry will never be greater than the frequency word, thus limiting the range of reference clock periods by which the carry is delayed.

As the frequency word approaches zero, the carry delay is always eight; however, carries are infrequent and therefore phase bias approaches zero. As the frequency word approaches $2^{32}-1$, carries occur frequently, but the carry delay approaches the correct number of reference clock periods. This is proved by substituting 2^{32} for FW into the equation showing the ideal carry delay algorithm, as follows:

$$(6) \quad Dcarry = INT (8 \times (1 - AW/2^{32}))$$
$$= INT (8 - AW/2^{29})$$
$$= 8 - INT (AW/2^{29})$$

The phase bias as a function of the frequency word caused by approximating the carry delay is given below:

$$(7) \quad PBcda = \frac{-PAcarry \times FW \times (FW/2^{32} - 1)}{2^{33}}$$

where PBcda is the phase bias as a result of the carry delay approximation. FIGURE 13 illustrates this bias.

This phase bias does not degrade closed loop tracking performance. However, it may be important to consider for measuring absolute phase of a signal (for example to generate a precision time mark) or for measuring the relative phase between two signals when the difference between their doppler is significant.

To setup initial phase of the code clock, the host processor provides the initial state of the state machine and the initial value of the thirteen most significant bits of the accumulator. The remaining nineteen bits of the accumulator are set to zero when a new code phase takes effect.

Since the state machine has either six or eight discrete states, each state represents a range of phase. Since state 100_2 is the state where the clock output changes from zero to one, this state represents an average phase of zero degrees. The range of phase it represents is -30 to +30 degrees for the 57.792 MHz plan and -22.5 to +22.5 degrees for the 40.9216 and 40.9200 MHz plans.

FIGURES 18 and 19 illustrate the phase range of each state for the 57.792 MHz plan and the 40.9216 and 40.9200 MHz plans respectively. In other words, instantaneous phase is a function of what state the state machine is in and the value held in the accumulator. Assuming the average value held in the accumulator is 2^{31} (half of the maximum value), then phase is expressed by the following equation:

$$(8) \quad Pcdclk = 360 \times \frac{S}{NS} + PAcarry \times \left[\frac{AW}{2^{32}} - \frac{1}{2} \right]$$

where Pcdclk is the code clock phase, NS is the number of states in the state machine, S is the state of the state machine, and AW is the value of the word in the accumulator at any time. S=O is defined as the state where the code clock goes high and all remaining states are numbered sequentially going counter clockwise (see FIGURES 5, 6 and 7).

For a desired phase, the host processor provided phase word can be calculated from the following equations. The initial state of the state machine, S, is calculated first using the following equation:

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$$(9) \qquad S = MOD \left\{ INT \left[\frac{NS \times Pcdclk}{360} + \frac{1}{2} \right], NS \right\}$$

where NS is the number of states in the state machine, Pcdclk is the desired code clock phase (must be positive) and S is the state that the state machine must be initialized to. After S is calculated, AW is calculated using the following equation:

$$(10) \qquad AW = 2^{n} \times MOD \left[\frac{Pcdclk}{PAcarry} - \frac{360 \times S}{PAcarry \times NS} + \frac{1}{2} + 8, 1 \right]$$

where PAcarry is phase advance per carry (see FIGURE 8) and AW is the value the adder/accumulator must be initialized to. In this equation, eight is added to force the value of the expression to be positive before taking the modulo. The phase word which the host processor must write out is a function of the initial state of the state machine, S, and the initial state of the adder/accumulator, AW. the three most significant bits of the phase word determine the initial state of the state machine.

FIGURE 8A shows the value of the three most significant bits of the phase word as a function of S for all setups. This is derived directly from FIGURES 5, 6 and 7 which show the state assignements for the state machine for each frequency plan. The thirteen least significant bits of the phase word determine the initial state of the thirteen most significant bits of the accumulator; the remaining accumulator bits are set to zero. The following equation shows the value of the thirteen least significant bits of the phase word as a function of AW:

$$(11) \qquad PW \; (13 \; lsbs) = INT \left[\frac{AW}{2^{19}} \right]$$

A more direct way to calculate the phase word involves using a simple equation and then modifying the result as required. The equation is:

$$(12) \qquad PW = MOD \left[\frac{Pcdclk}{360} + \frac{1 + NS}{2 \times NS}, 1 \right] \times \frac{NS}{8} \times 2^{16}$$

Then the result is modified as follows:
– IF PAcarry < 0 THEN PW = PW EXOR 8191 (invert 13 least significant bits)
– If NS = 6 AND PW ≧ 24576 THEN PW = PW + 8192
This yields the final phase word for the host processor to write out.

During the development of this invention, a problem was found in that the phase is not always finally settable. There are phase settability anomalies depending upon the frequency to which the digital oscillator is set. A description of this problem follows.

Code clock average phase is calculated based on the assumption that the average value of the adder/accumulator during a sample integration period is half the maximum value possible (a previous assumption). This is not true in all cases. Code clock phase is actually calculated using the following equation for all cases:

$$(13) \qquad Pcdclk = 360 \times \frac{S}{NS} + PAcarry \times \left[\frac{AW - AA}{2^{32}} \right]$$

where AA is the average value of the adder/accumulator for a sample integration period.

The average value of the adder/accumulator for a sample integration period is a function of the frequency word and the initial state of the adder/accumulator and is calculated using the following equation:

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$$(14) \qquad AA = \frac{1}{N} \sum_{i=0}^{N} MOD(AW + i \times FW, 2^{32})$$

where N is the number of times the adder/accumulator is incremented in a sample integration period.

For most frequency words, as N approaches infinity, the average adder/accumulator value is very close to 2^{31} and is not effected by the initial adder/accumulator value (AW). However, certain specific frequency words cause the average adder/accumulator value to be a function of the initial adder accumulator value. When this occurs, a phase settability anomaly occurs.

The frequency words which cause a phase settability anomaly, and the degree to which phase settability is effected can be determined as follows:

1) Reduce the following fraction as much as possible:

$$(15) \qquad \frac{n}{d} = \frac{FW}{2^{32}}$$

where n is the numerator of the reduced fraction and d is the denominator of the reduced fraction.

2) Phase settability is calculated by the following equation:

$$(16) \qquad P_{stby} = \frac{360}{NS \times d}$$

where P_{stby} is the phase settability and NS is the number of states in the state machine.

For example, when the frequency word is zero (n=0 and d=1), the adder/accumulator remains at its initial state for the entire sample integration period, thus AA = AW. When AW is substituted for AA in the equation 14, then code clock phase is no longer a function of the initial adder/accumulator value, but only of the initial state of the state machine. This causes a phase settability anomaly, which when the frequency word is zero, does not allow phase settability to a finer resolution than 360 divided by the number of states in the state machine (45° for the 40.9200 and 40.9216 MHz plans and 60° for the 57.792 MHz plan).

Other frequency words will result in a finite number of discrete adder/accumulator values evenly spaced apart. For example, if the frequency word is 2^{31} (n=1 and d=2) then the value held in the adder/accumulator at any time is one to two values:

$$(17) \qquad AW \text{ or } MOD(AW + 2^{31}, 2^{32}).$$

In this case the average value of the adder/accumulator is:

$$(18) \qquad AA = \frac{AW + MOD(AW + 2^{31}, 2^{32})}{2}$$

Thus another phase settability anomaly occurs when the frequency word is 2^{31} in which the phase settability is:

$$(19) \qquad Pstby = \frac{360}{NS \times 2}$$

(22.5° for the 40.9200 and 40.9216 MHz plans and 30° for the 57.792 MHz plan).

FIGURE 14 shows the phase settability for all values of d which yield a phase settability of 2 degrees or greater.

FIGURES 15, 16 & 17 graph these phase settability anomalies with normal code clock generator operating range super-imposed for the 57.792 MHz plan, the 40.9216 MHz plan and the 40.9200 MHz plan, respectively. Values of d which are not binary multiples are not strictly attainable; however, since the sample integration period is not infinite, values for d which are not a binary multiple are effectively attainable.

Turning now to FIGURE 10, carrier generator 109 creates an inphase (I) and quadrature (Q) replica of the L1 or L2 intermediate frequency (IF) carrier signal. The output of the carrier generator, called carrier, is generated synchronous to the reference clock. The inphase (I) and the quadrature (Q) parts of the carrier are each two bits. Phase and frequency of the carrier is programmable via the host processor.

FIGURE 12 shows the frequency range, frequency settability, and phase settability for the three reference clock frequencies supported by the PCOAC.

The carrier is generated using the same principle as is used for generating the code clock. The state machine for the carrier generator operates using the same principle as for the code clock generator state machine. State assignments for the carrier generator are the same for all three PCOAC supported frequency

plans. The carrier phase advances 90° per reference clock and either +45° or -45° per adder/accumulator carry. The 45° phase advance or retard per carry (PAcarry) is controlled by a high/low frequency control bit.

FIGURE 11 shows the complex carrier output as a function of state. Note that the state machine generates a 2-bit number for each part of the complex carrier at each state. These two bit numbers can either be a -2, -1, +1 or +2. The host processor can set a bit which hard limits the output to +1 and -1. The quadrature carrier lags the inphase carrier by 90 degrees.

The adder/accumulator for the carrier generator is exactly the same as for the code clock generator.

The average frequency of the carrier output is calculated as follows:

$$(20) \qquad FCarrier = \frac{Fref}{360} (90 + \frac{FW}{2^{35}} \times PAcarry)$$

where Fcarrier is average frequency of the carrier, Fref is the reference clock frequency, FW is the 32-bit frequency word provided by the host processor and PAcarry is the phase advance per carry (+45 or -45).

The carry delay circuit for the carry generator is the same as it is for the code clock generator. The frequency depend phase bias caused by this delay circuit is calculated the same as for the code clock generator. Carrier phase is controlled the same way as code clock phase.

The state machine has eight states. Each state represents a phase range of 45 degrees. State 000 represents an average phase of 22.5 degrees. The range of phase which it represents is 0 to +45 degrees. Figure 20 illustrates the phase range of each state. Assuming the average value held in the accumulator is 2^{31} (half of the maximum value), the carrier phase is expressed by the following equation:

$$Pcarrier = 45 \times S + 22.5 + PAcarry \times \left[\frac{AW}{2^{32}} - \frac{1}{2} \right]$$

$$(21)$$

where Pcarrier is the carrier phase, S is the state of the state machine as defined in FIGURE 11, and AW is the current content of the adder/accumulator.

The host processor sets the initial state of the state machine and the thirteen most significant bits of the accumulator. For a desired phase, the phase word can be calculated from the following equations. The initial state of the state machine, S, is calculated first using the following equation:

$$S = MOD \left[INT \left[\frac{Pcarrier}{45} \right], 8 \right]$$

$$(22)$$

where Pcarrier is the desired carrier phase and S is the state that the state machine must be initialized to as defined in FIGURE 11. After S is calculated, AW is calculated using the following equation:

$$AW = 2^{32} \times MOD \left[\frac{Pcarrier}{PAcarry} + 8, 1 \right]$$

$$(23)$$

where PAcarry is the phase advance per adder/accumulator carry (-45 or +45 degrees) and AW is the value the adder/accumulator must be initialized to. In this equation, eight is added to force the value of the expression to be positive before taking the modulo. The phase word which the host processor must write out is a function of the initial state of the state machine, S, and the initial state of the adder/accumulator, AW. The three most significant bits of the phase word determine the initial state of the state machine. The thirteen least significant bits of the phase word determine the thirteen most significant bits of the accumulator; the remaining bits of the accumulator are set to zero. The following equation shows the phase word as a function of S and AW:

$$PW = S \times 2^{13} + INT \left[\frac{AW}{2^{19}} \right]$$

$$(24)$$

A more direct way to calculate the phase word involves using a simple equation and then modifying the result as required. For Pcarrier from 0° to less than 360°, the equation is:

$$(25) \qquad PW = 2^{16} \times \frac{Pcarrier}{360}$$

Then the result is modified as follows:

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IF PAcarry < 0 THEN PW = PW EXOR 8191 (invert 13 least significant bits)

There are two contributors to carrier phase settability anomalies, the adder/accumulator carry delay circuit and the unequal spacing of states due to having four output levels. Phase settability anomalies resulting from the carry delay circuit have been previously described. Only phase settability anomalies resulting from the unequal spacing of states will be described now.

The carrier generator state machine has eight states. Ideally these states would be evenly spaced 45 degrees apart. Because the carrier generator has four output levels (-2, -1, +1 and +2), the states are not evenly spaced.

FIGURE 21 shows an ideal spacing versus the actual spacing achieved with four output levels. As can be seen from the FIGURE, four states are on one set of orthogonal axes and the other four states are on another set of orthogonal axes. Each set of axes has a phase bias associated with it with respect to the ideal case. The phase bias associated with states 000_2, 010_2, 100_2 and 110_2 is 4.065 degrees and with states 001_2, 011_2, 101_2, and 111_2 is -4.065 degrees. Note, when carrier hard-limiting is enabled, the outputs are effectively evenly spaced alleviating the cause of this phase settability anomaly.

For most set-ups, the state machine will spend very close to half the time on each set of axes during an integration period, thus the biases cancel. However, some set-ups will cause the state machine to spend significantly more time on one set of orthogonal axes than on the other. Phase bias associated with a set-up is calculated using the following equation:

$$(26) \qquad P_{bias} = P_e \times 8.130 - 4.065$$

Where P_{bias} is the phase and P_e is the percentage of time the state machine dwells on an even state (000_2, 010_2, 100_2 or 110_2) during an integration period. This phase bias, unless compensated for, causes a phase settability anomaly.

Frequencies which cause phase settability anomalies are ones which cause the state machine to dwell a significantly different percentage of the time on one set of orthogonal axes than on the other. The carrier generator state machine only changes the set of axes it is on when the adder/accumulator carries. Therefore, frequency words which cause this type of phase settability anomaly are the ones which cause the adder/accumulator to carry an even number of times every odd number clocks. For example, if the adder/accumulator carries twice every five clocks, then two out of every five clocks (40 percent of the time) the state machine will be on one set of axes and three out of every five clocks (sixty percent of the time) the state machine will be on the other set of axis. This results in a phase bias of +/-0.813 degrees, or a phase settability anomaly of 1.626 degrees. Only two frequency words cause this type of phase settability anomaly to be greater than 2 degrees. A frequency word of zero causes a phase settability anomaly of 4.07 degrees and a frequency word of $2/3 \times 2^{32}$ causes a phase settability anomaly of 2.71 degrees.

FIGURE 22 shows all phase anomalies greater than 2 degrees for the carrier generator as a function of the frequency word. Super-imposed on this graph, is the normal operating range for the carrier generator for each mode of operation.

This design approach can benefit any system where power conservation is important and where a high precision digital oscillator is required whose output must be synchronous to a high speed clock. The more bits of precision required and the higher the frequency of the reference clock, the greater the power savings over a conventional adder/accumulator digital oscillator approach.

FIGURE 29 shows a block diagram of the intermediate correlator module 202 (FIGURE 2). Each of the eight complex correlators per channel in the PCOAC includes four six bit adder/accumulators, two for in phase accumulation and two for quadrature accumulation. The adder/accumulators function in pairs, one to accumulate positive values and one to accumulate negative values. In addition to the 32 adder/accumulators required per channel for the eight correlators, two adder/accumulators are required per channel to support the noise meter, making a total of 68 adder/accumulators on the chip running at up to 57.792 MHz. This makes power dissipation an issue. Using asynchronous design techniques one of these adder/accumulators takes less than 60 gates and dissipates less than 7 mW. A conventional ripple-adder with a 6-bit register, takes about 90 gates and dissipates about 25 mW.

FIGURE 23 shows the block diagram of a conventional adder/accumulator, while FIGURE 24 shows the block diagram of the specially developed adder/accumulator. For 68 adder/accumulators, this is a difference of almost 2,000 gates and, for a system with six complete L1 and L2 channels, this is a difference of about 6.8 watts. Permutation is used elsewhere in the PCOAC and is discussed later. This adder/accumulator is the most significant of many design innovations that make the PCOAC possible.

The implementation of intermediate correlator module 202 (FIGURE 2) requires the development of three custom macro-cells, which are combined to form a hard-macro function called ICORR. These three custom macro-cells are:

– the BIADD6, the aforementioned 6-bit adder/accumulator (binary multiple only),

– the PULGENA, a pulse generator to drive the two BIADD6s for noise measurements, and

– the PULGENB, a pulse generator to drive a group of sixteen BIADD6s associated with four correlators.

The BIADD6 is a 6-bit adder/accumulator designed for low power operation and low gate utilization. It is implemented using a ripple counter 2402 with a boolean exclusive OR between each stage 2401. (FIGURE 24)

FIGURE 25 shows a standard 6-bit ripple counter with a clear direct input. FIGURE 26 shows this same ripple counter with a transmission gate exclusive OR 2603, 2605, 2607, 2609, 2611 between each stage 2502, 2503, 2504, 2505, 2506, 2507 and with the input data gated with a pulse input 2601, 2602, 2604, 2606, 2608, 2610.

FIGURE 27 shows the same function as FIGURE 26 but with the transmission gate exclusive ORs replaced with boolean exclusive ORs, 2702 and 2708. These exclusive ORs are used to inject a pulse to any stage of the ripple counter. Boolean exclusive OR gates are required because transmission gate exclusive OR gates which are available produce a glitch which affects circuit operation. The content of the ripple counter is the accumulated value. When the clock input to one of the toggle flip/flops (which comprise the ripple counter) is pulsed, the value 2^n is added to the accumulated values where n (0 to 5) indicates which flip/flop input is pulsed.

FIGURE 28 shows the final implementation of the BIADD6 macro-cell. Ripples start from either edge of an injected pulse depending upon the state of the previous flip/flop. The worst case ripple through the BIADD6 is when the BIADD6 contains a 111110_2 and a 2 is added followed by adding a 32. When this occurs, the second flip/flop is clocked on the falling edge of the first injected pulse and the sixth flip/flop is clocked on the rising edge of the second injected pulse. Therefore, the BIADD6 must ripple from the second flip/flop to the last flip/flop during the pulse low time (significantly less than one reference clock period). To provide more margin, negative edge clocking flip/flops are used to reduce propagation delay for a ripple and pulse injection to the last stage is delayed 2807 in order to give more time for a worst case ripple. A pulse generator is also used to provide a short positive going pulse, which also provides more time for the worst case ripple. There are two pulse generators, PULGENA and PULGENB.

PULGENA is a custom macro-cell designed to provide short high going pulses for the two BIADD6 cells allocated to the noise meter. FIGURE 31 shows the PULGENA custom cell. The pulse generator works by AND-ing 3106 and 3107 the reference clock with a delayed and inverted version of the reference clock 3103, 3104 and 3105 and with the sign bit for the next sample of noise data. PULGENA has two sign inputs, one active high and the other active low. It also has an off input which forces the delayed reference clock low, thus masking the pulse outputs. A great deal of SPICE insulation was required to verify the width of the pulse generated is never too narrow to be missed by the BIADD6 and is always narrow engough to guarantee the worst case ripple through the BIADD6.

PULGENB is a custom macro-cell designed to provide short high going pulses for sixteen BIADD6 cells allocated to one set of four correlators. FIGURE 10 shows the PULGENB custom cell. One pulse generator is used for all sixteen BIADD6s for power conservation. The PULGENB is designed using the same principle as the PULGENA.

The BIADD6 custom cell architecture requires that only certain inputs be used, primarily binary multiple only inputs.

FIGURE 32 lists the valid inputs for the BIADD6 in all applications.

FIGURE 33 shows an example of how two BIADD6 cells are used together to perform the high frequency integration.

FIGURE 37 shows inputs which are always invalid and will cause the BIADD6 to operate in a way that is unpredictable.

Lastly, FIGURE 35 shows inputs which may produce determinant results depending on the values that are already contained in the BIADD6 circuit. These input values yield determinant results when the following two criteria are met. Two adjacent bits of the adder/accumulator cannot be added to during the same reference clock period, and the bit adjacent to and less significant than a bit being added to cannot be carried into during the same reference clock period.

By modifying the BIADD6 cell slightly, it is possible to make an adder/accumulator which is not restricted to adding only binary-multiples. To do this, the boolean logic exclusive OR must have a balanced rise and fall time and the whole adder accumulator must have time to settle between clock edges (both the rising and falling edges are active).

Asynchronous pulses occur at the output of these boolean logic EXORs when the data input to the EXOR is pulsed and the previous flip-flop carries. A balanced rise and fall time of the EXOR ensures that this pulse will meet the minimum pulse width requirement for the flip/flop. FIGURE 36 shows the transistor level model of the boolean EXOR used in a previously developed experimental ASIC. Two P transistors are used in parallel to balance the N transistors. The technology used for the PCOAC has balanced P and N transistors, therefore

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the boolean EXOR in the PCOAC has only four P transistors.

FIGURE 37 shows the special adder/accumulator cell developed for the PCOAC. It uses a 2-to-1 multiplexer 3702 to give the adder/accumulator two ports. Using an N-to-1 multiplexer in a similar manner would expand the operation of the adder/accumulator cell to N ports.

FIGURE 38 shows how these cells are connected together to create a 4-bit adder/accumulator. To add margin for reliability, delay 3802, 3803, and 3804 are added between stages 3701. The flip-flop 3808, 3809, 3810 are used to pipeline the carry between adder/accumulator stages.

FIGURE 39 shows a 32-bit adder/accumulator built by pipelining 4-bit adder/accumulators together. Referring back to FIGURE 38, after each complete addition, the most significant bit 11 of a 4-bit adder/accumulator is clocked into register 3808. The clock 12 used for this operation is called the carry clock. The bit is then clocked into another register using the opposite edge of the carry clock. A delayed version of the carry clock 13 clocks this bit a third time to propagate it to the carry input of the least significant bit of the next stage just after the addition at that stage has been started. It is necessary to use a delayed version of the carry clock to ensure that the carry is not injected too soon thus violating the minimum pulse width requirement of the least significant toggle flip-flop.

This 32-bit adder/accumulator 3901 is used four times in the PCOAC, once in each code clock generator (FIGURE 4) and once in each carrier generator. In addition, a non-pipelined adder/accumulator uses the special adder/accumulator cell 3701 (FIGURE 37) for implementing part of the search processor circuitry 206 (FIGURE 2). This adder/accumulator configuration saves gates over a conventional adder/accumulator.

We are now going to discuss circuitry contained within the back end correlator module 203 of FIGURE 2. In order to perform predetection integration in the back end correlator module, it is prior art to use synchronous up/down counters. In a previous development, it was found that ripple counters could be used which would either count up 1 or not count at all. Two ripple counters would be used for each correlator, one for inphase integration, and one for quadrature integration. A separate counter common to all correlators in a channel, was kept to keep tract of how many reference clocks were generated during an integration period. At the end of an integration, the number of reference clocks or accumulated bias is subtracted from the final value accumulated for each in-phase and quadrature integrator.

This circuit had to be modified for two reasons. The first reason is that the circuit supports full null zone which means that the value in the chip of the demodulated signal is no longer just +1 or -1, but has multiple possible input valves. Secondly, in order to support search, we perform adjacent correlator presuming, and this removes the signal to noise ratio holes between correlators.

FIGURE 40 shows a block diagram of the back end correlator module 203 from FIGURE 2. The problems previously mentioned are solved in the sample accumulators 4101 of FIGURE 41. The carries from the intermediate correlator module enter the sample accumulators and are immediately divided down by 8, 4107 and 4108, and are then reclocked 4109, 4110 and edge detection is performed, 4111 and 4112. Re-clocking occurs prior to edge detection in order to reduce the chance that a meta-stable state might effect a final accumulation value. From the output of the edge detector pulses are encoded 4113.

FIGURE 42 shows the translation from carries from the intermediate correlator to which pulses are encoded. The pulses are encoded in such a way that a bias of 1 is added on every clock. The output of the pulse encoder will either be nothing, a pulse with a value of 1, or a pulse with the value of 2. These pulses go into a 22-bit ripple counter 4114, whose first stage uses the adder/accumulator technique previously mentioned so that a 1 or a 2 can be added. A separate bias accumulator 4106 is kept which keeps track of reference clocks or how many times the +1 value is added. At the end of each integration a 22 bit 16:1 multiplexer 4104 selects each accumulated value and substracts the bias off using the adder 4105. These values are stored in the I&Q RAM 204 and 205 of FIGURE 2. FIGURE 43 shows the detailed circuitry required to build a sample accumulator as previously described. For search applications, the search processor previously described and also described in the above-mentioned copending patent application entitled "System and Method for a Digital Navigation Satellite Receiver" uses all correlators to search for the signal.

FIGURE 45 shows the relative signal to noise ratio as a function of code error or how far the incoming signal is away from the signal generated in the chip at a particular correlator. As can be seen in this FIGURE, there is a 2.5 dB signal to noise ratio hole between each of the correlators which are spaced 0.5 chips apart. To eliminate this hole, adjacent correlator values are summed together FIGURE 44. This process is called adjacent correlator presumming. It is called presumming because it is done during predetection integration. The adder/accumulators support this, as shown in FIGURE 43.

FIGURE 46 shows the results of adjacent correlator presumming. As can be seen, there is a flat 1.25 dB loss, but there are no signal to noise ratio holes. Our sample accumulator/circuit accomplishes this, as shown in FIGURE 43, by taking the pulses encoded from the adjacent correlator and applying those values to the 22 bit accumulator 4114. In doing this, the correlator controller must clock the bias accumulator 4106 of FIGURE

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41 at twice its normal rate, as noted at the bottom of FIGURE 41.

Although this description describes the invention with reference to the above specified embodiments, the claims and not this description limit the scope of the invention. Various modifications of the disclosed embodiment, as well as alternative embodiments of the invention, will become apparent to persons skilled in the art upon reference to the above description. Therefore, the appended claims will cover such modifications that fall within the true scope of the invention.

Claims

1. A device for use in GPS receivers for processing of multiple digitzed satellite signals, said device comprising:
   multiple L1/L2 P(Y) and C/A-code channels on a single application specific integrated circuit (ASIC); and
   a search processor for fast signal acquisition.

2. The device set forth in claim 1 further including:
   circuitry for tracking said C/A and P(Y)-code simultaneously.

3. The device set forth in claim 1 further including:
   circuitry for processing P-code or Y-code selectively.

4. The device set forth in claim 1 wherein said Y-code is generated by a single Y-code generator common to all said multiple channels.

5. The device set forth in claim 1 further including:
   circuitry for selectively processing said L1 or L2 signals.

6. The device set forth in claim 1 further including:
   circuitry for supporting full null zone signal inputs.

7. The device set forth in claim 1 further including:
   a digital oscillator for providing carrier or code clock synchronous to a high frequency reference clock.

8. The device set forth in claim 1 further including:
   an adder/accumulator primarily for accumulating only binary multiples, said adder/accumulator including:
   pulse injectors operating in conjunction with a ripple counter for reducing power and gate count.

9. The device set forth in claim 1 further including:
   a correlator configuration using ripple counters for predetection integration and bias accumulation; and
   an adder for substraction of said bias.

10. The method of operating a circuit in a global positioning system (GPS) receiver, said method comprising the steps of:
    by digital signal processing on a single integrator circuit (IC):
    acquiring or tracking valid P-code signals from at least one satellite of said GPS.

11. The method set forth in claim 10 wherein said acquiring or tracking step includes the step of:
    processing C/A code.

12. The method set forth in claim 11 wherein said tracking step includes the step of:
    tracking C/A and P-code simultaneously.

13. The method set forth in claim 10 wherein said acquiring or tracking step includes the step of:
    processing P-code or Y-code selectively.

14. The method set forth in claim 13 wherein said acquiring or tracking step includes the step of:
    processing multiple channels.

15. The method set forth in claim 14 wherein said Y-code on any said channel is generated by a single Y-code generator common to all said multiple channels.

16. The method set forth in claim 10 wherein said acquiring or tracking step includes the step of: processing multiple channels.

17. The method set forth in claim 10 further comprising the step of: selectively processing L1 or L2 signals.

18. The circuit for use in a global positioning system (GPS) receiver, said circuit comprising: digital signal processing (DPS) circuitry on a single integrated circuit (IC) for acquiring or tracking valid P-code signals from at least one satellite of said GPS.

19. The circuit set forth in claim 18 wherein said DSP includes circuitry for processing C/A code.

20. The circuit set forth in claim 19 wherein said DSP includes: circuitry for tracking C/A and P-code simultaneously.

21. The circuitry set forth in claim 18 wherein said DSP includes circuitry for processing P-code or Y-code selectively.

22. The circuitry set forth in claim 18 wherein said DSP includes circuitry for supporting full null zone signal inputs.

23. The circuitry set forth in claim 18 wherein said DSP further includes a digital oscillator for providing carrier or code clock synchronous to a high frequency reference clock which mostly runs at a significantly lower frequency for reduced power dissipation.

24. The circuitry set forth in claim 23 wherein said digital oscillator for carrier generation includes circuitry for selective one or two bit carrier generation.

25. The circuitry set forth in claim 18 wherein said DSP further includes:
an adder/accumulator primarily for accumulating only binary multiples, said adder/accumulator including:
pulse injectors operating in conjunction with a ripple counter for reduced power dissipation and gate count.

26. The circuitry set forth in claim 18 wherein said DSP further includes:
a correlator configuration including ripple counters for predetection integration bias accumulation; and an adder for subtraction of said bias.

27. A digital oscillator for providing a clock synchronous to a high frequency reference, said oscillator comprising:
a low frequency adder/accumulator;
a carry delay circuit;
a high frequency state machine; and
circuitry for interactively controlling said adder/accumulator, said carry delay circuit and said state machine.

28. An adder/accumulator for low power operation comprising:
an adder/accumulator primarily for accumulating only binary multiples, said adder/accumulator including:
pulse injectors operating in conjunction with a ripple counter for reducing power and gate count.
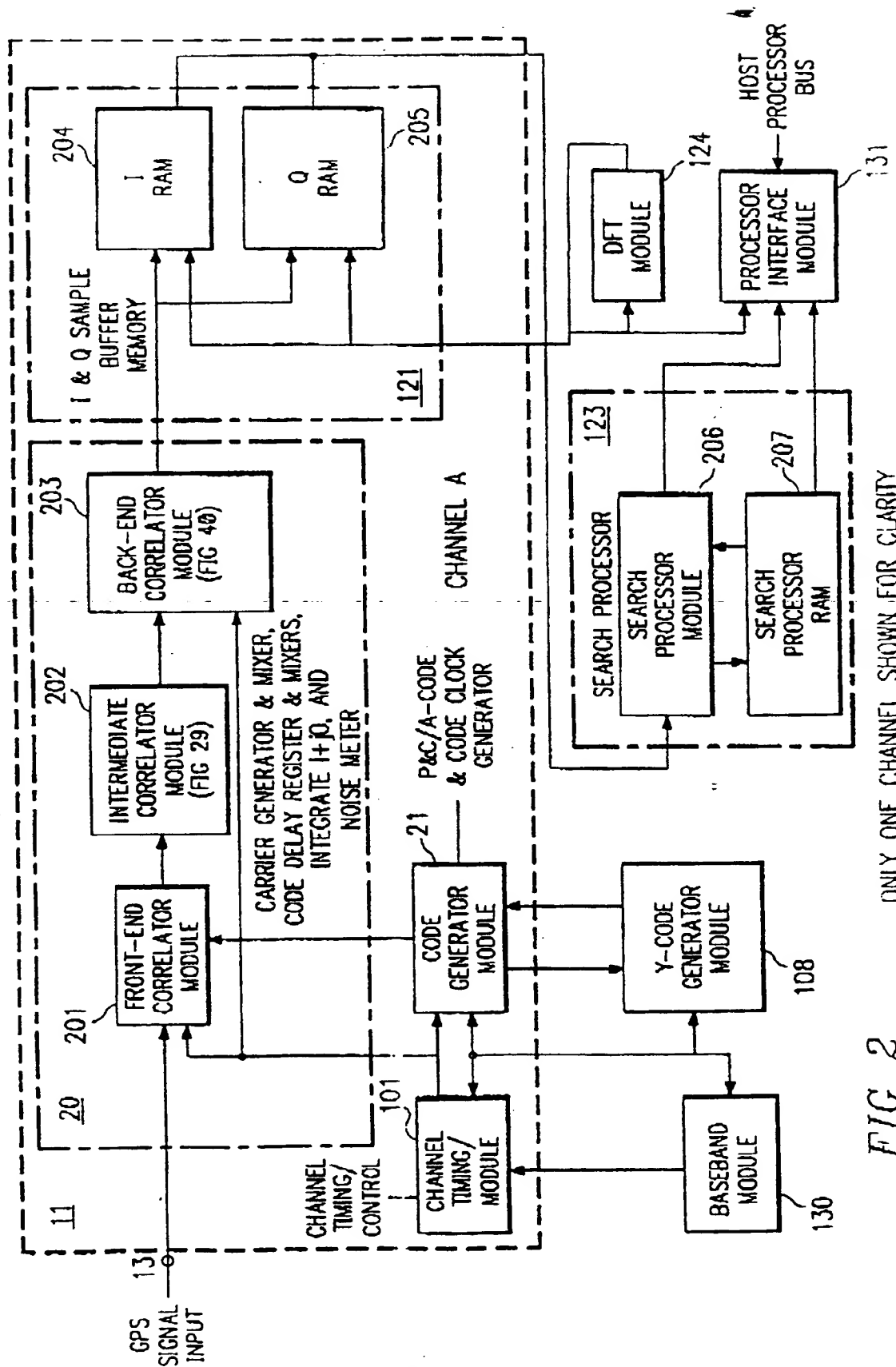
14

FIG. 1
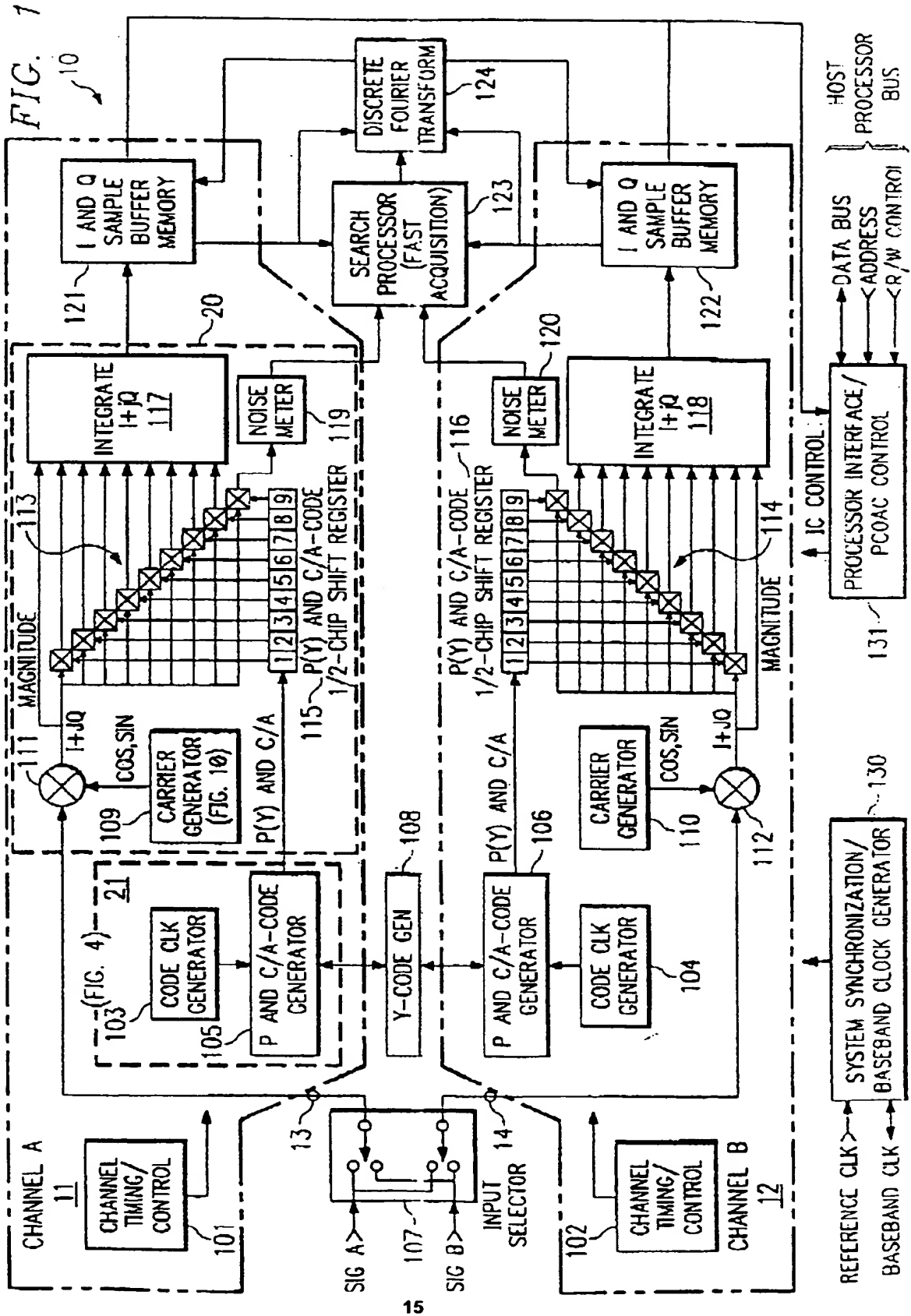
FIG 2

ONLY ONE CHANNEL SHOWN FOR CLARITY

FIG 3
(PRIOR ART)
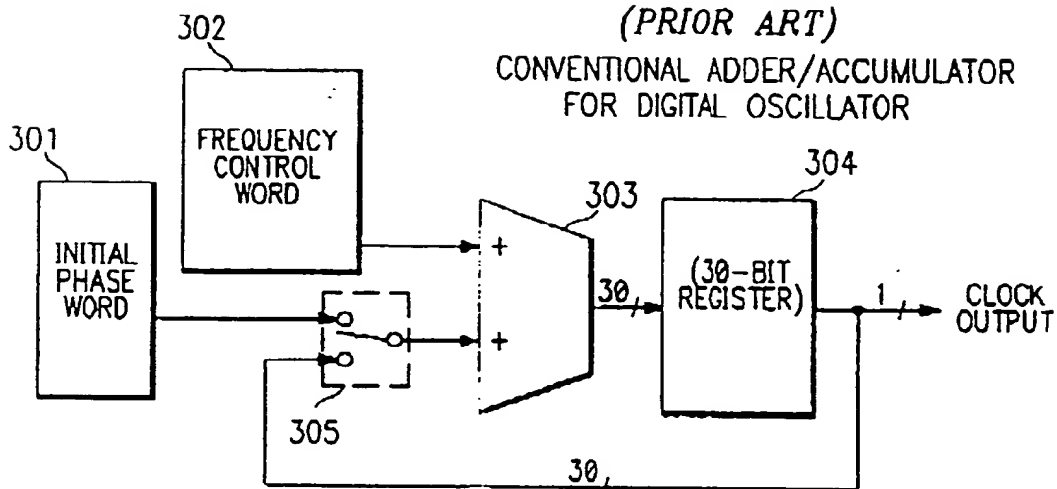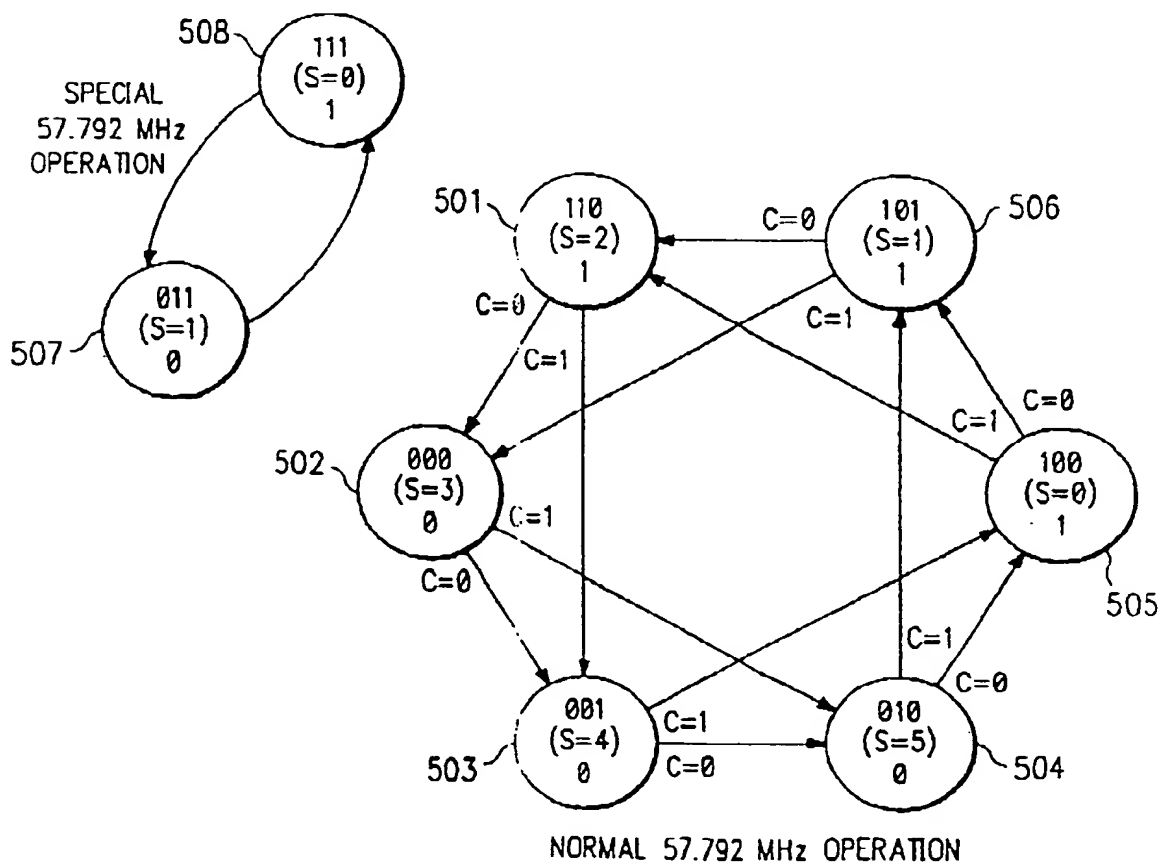CONVENTIONAL ADDER/ACCUMULATOR
FOR DIGITAL OSCILLATOR

FIG. 5

CODE CLOCK STATE DIAGRAM FOR 57.792 MHz PLAN

SPECIAL
57.792 MHz
OPERATION

NORMAL 57.792 MHz OPERATION

FIG 4

CODE CLOCK GENERATOR — 103

CODE CLOCK OUTPUT

Fs — 408 — CODE CLOCK GENERATOR STATE MACHINE

Fs

DELAY CARRY BY: 7 – (3MSBs) REFERENCE CLOCK PERIODS. — CARRY DELAY CIRCUIT — 407

3 MSBs

3901

32 — 32 BIT REG — 406 — Fs/B

32 — 405 — 32 BIT ADDER — ADDER/ACCUMULATOR

32 — 404

13 LSBs — ACTIVE FREQUENCY WORD — FIG 39

3MSBs

3 BIT LATCH — 409 — 3

3905 — 13 BIT LATCH — 13 — 3902

32 BIT LATCH — 32

32 BIT LATCH — 32

NEXT PHASE WORD

NEXT FREQUENCY WORD — 3904 — ACTIVE FREQUENCY WORD

FIG. 8a

THE THREE MOST SIGNIFICANT BITS OF THE PHASE WORD AS A FUNCTION OF S.

PHASE WORD 3 MSBs	VALUE OF S		
	57.7920 MHz NORMAL	40.9216 OR 40.9200 MHz	57.792 MHz SPECIAL
4	0	0	N/A
5	1	1	N/A
6	2	2	N/A
7	N/A	3	0
0	3	4	N/A
1	4	5	N/A
2	5	6	N/A
3	N/A	7	1

FIG. 8

STATE MACHINE OPERATION VERSUS FREQUENCY PLAN

REFERENCE CLOCK FREQUENCY (MHz)	CODE CLOCK PHASE ADVANCE PER REFERENCE CLOCK (DEGREES)	CODE CLOCK PHASE ADVANCE PER CARRY (DEGREES)
57.7920	+60	+60
40.9216	+90	-45
40.9200	+90	-45 OR +45

18

FIG. 6

CODE CLOCK STATE DIAGRAM
FOR 40.9216 MHz PLAN
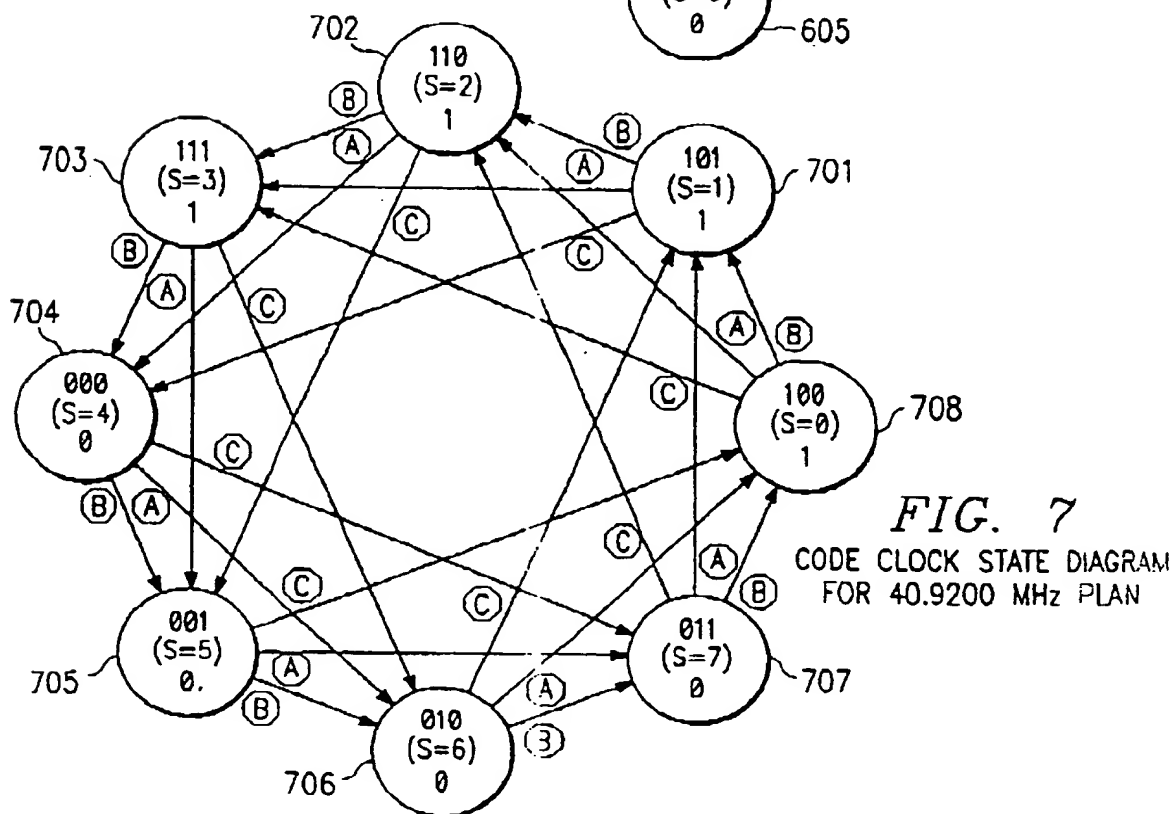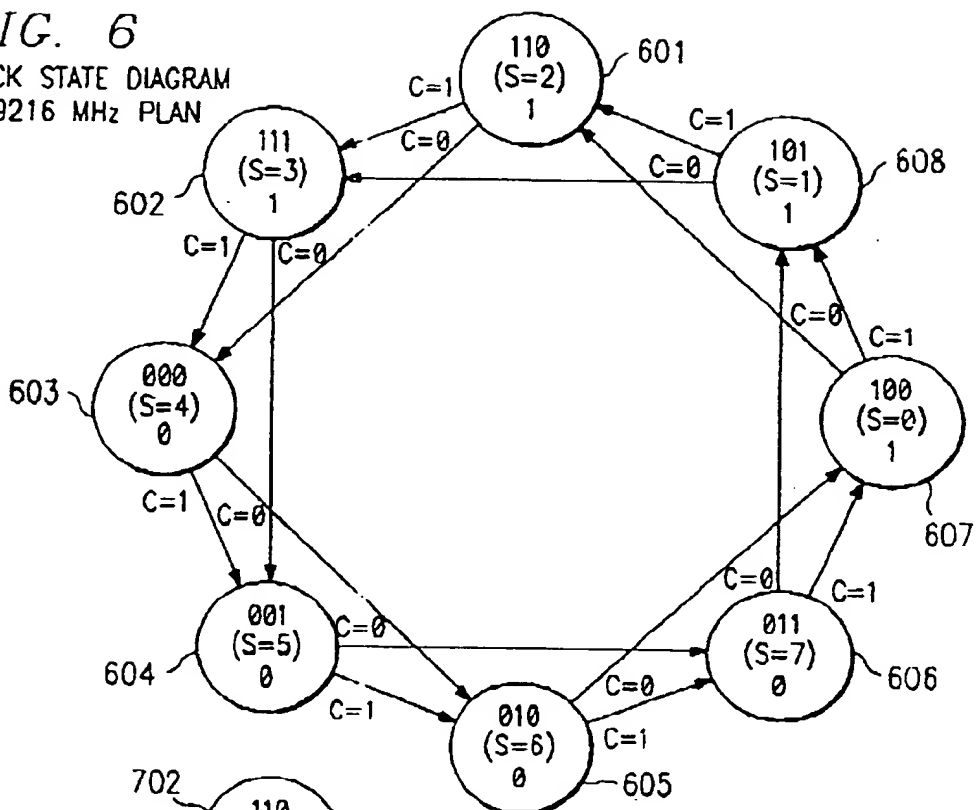
FIG. 7

CODE CLOCK STATE DIAGRAM
FOR 40.9200 MHz PLAN

A — NO CARRY
B — CARRY AND HIGH/LOW BIT SET LOW (<10.23 MHz)
C — CARRY AND HIGH/LOW BIT SET HIGH (>10.23 MHz)

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FIG 10

FIG. 9

CLOCK OPERATION vs. FREQUENCY PLAN

REFERENCE CLOCK FREQUENCY (MHz)	FREQUENCY RANGE (MHz)	FREQUENCY SETTABILITY (Hz)	PHASE SETTABILITY (DEGREES)
57.7920	9.6320 to 10.8360	0.000280328	0.00732422
40.9216	9.5910 to 10.2304	0.000148872	0.00549316
40.9200	9.5907 to 10.8693	0.000148866	0.00549316

FIG. 12

SUMMARY OF OPERATION VERSUS FREQUENCY PLAN

REFERENCE CLOCK FREQUENCY (MHz)	FREQUENCY RANGE (MHz)	FREQUENCY SETTABILITY (Hz)	PHASE SETTABILITY (DEGREES)
57.7920	13.5450 to 15.3510	0.000210246	0.00549316
40.9216	9.5910 to 10.8698	0.000148872	0.00549316
40.9200	9.5907 to 10.8693	0.000148866	0.00549316

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FIG. 11

CARRIER GENERATOR STATE DIAGRAM

A — NO CARRY
B — CARRY AND HIGH/LOW BIT SET LOW
C — CARRY AND HIGH/LOW BIT SET HIGH
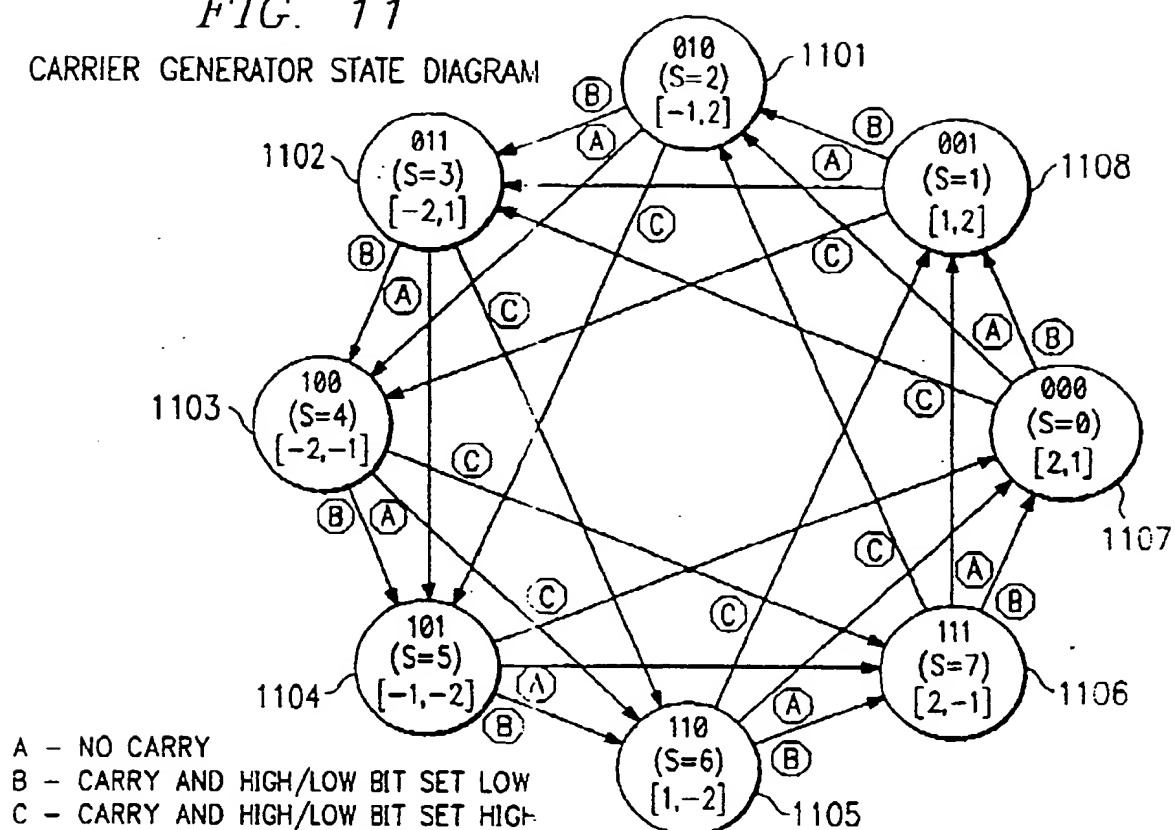
FIG. 13

CARRY DELAY APPROXIMATION PHASE BIAS

PHASE BIAS (DEGREES)
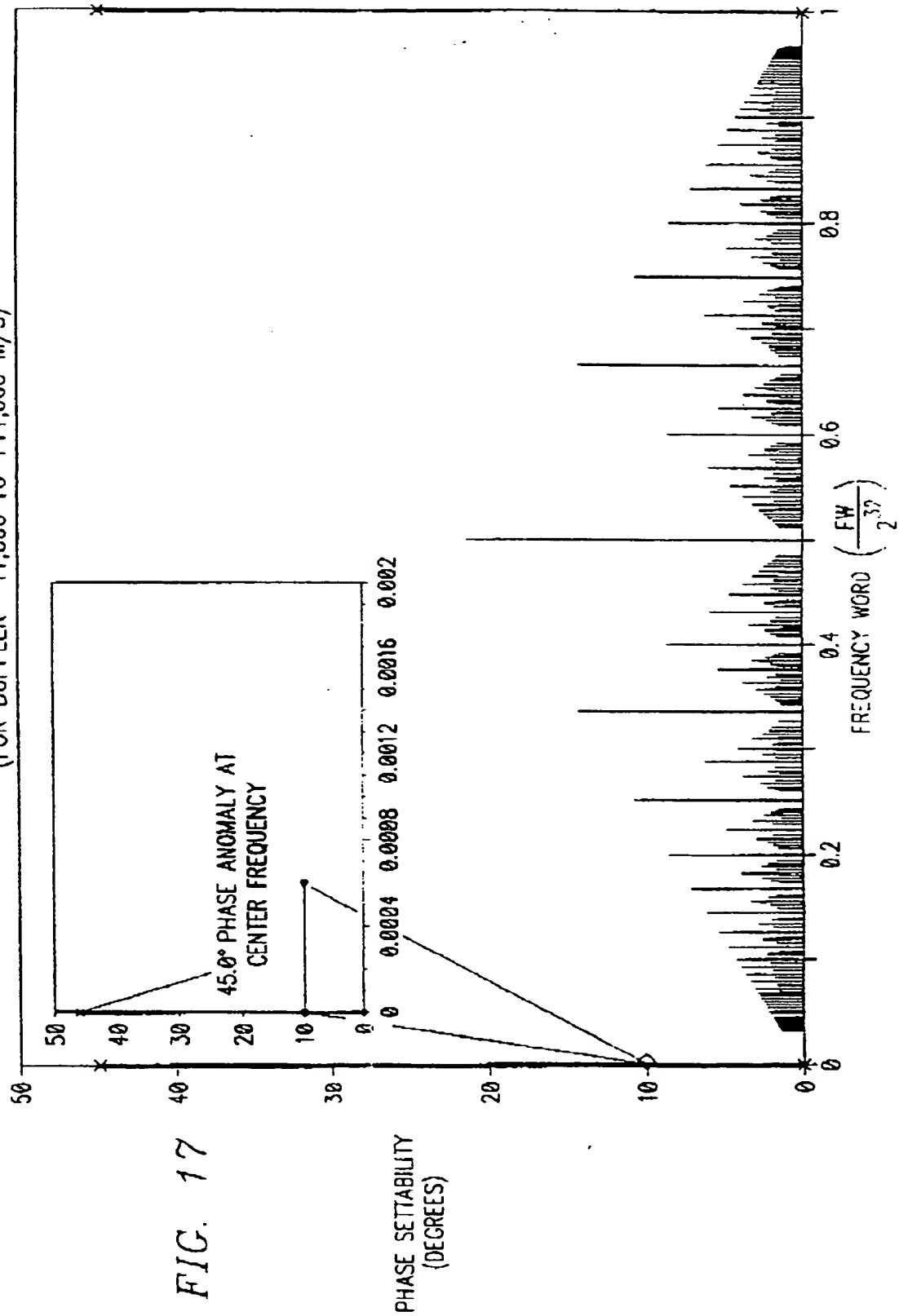
PAcarry = −45°

PAcarry = +45°

PAcarry = +60°

FREQUENCY WORD $\left(\dfrac{FW}{2^{32}}\right)$

21

FIG. 18
PHASE RANGE OF EACH STATE IN 57.792 MHz PLAN

+90°

+150° 110 (S=2) 1   101 (S=1) 1   +30°

000 (S=3) 0   100 (S=0) 1

001 (S=4) 0   010 (S=5) 0

+210°   -30°

+270°

▨ REGION WHERE X1 MUST BE INCREMENTED BY
BECAUSE FIRST RISING EDGE OF A NEW SET-UP
DOES NOT OCCUR.
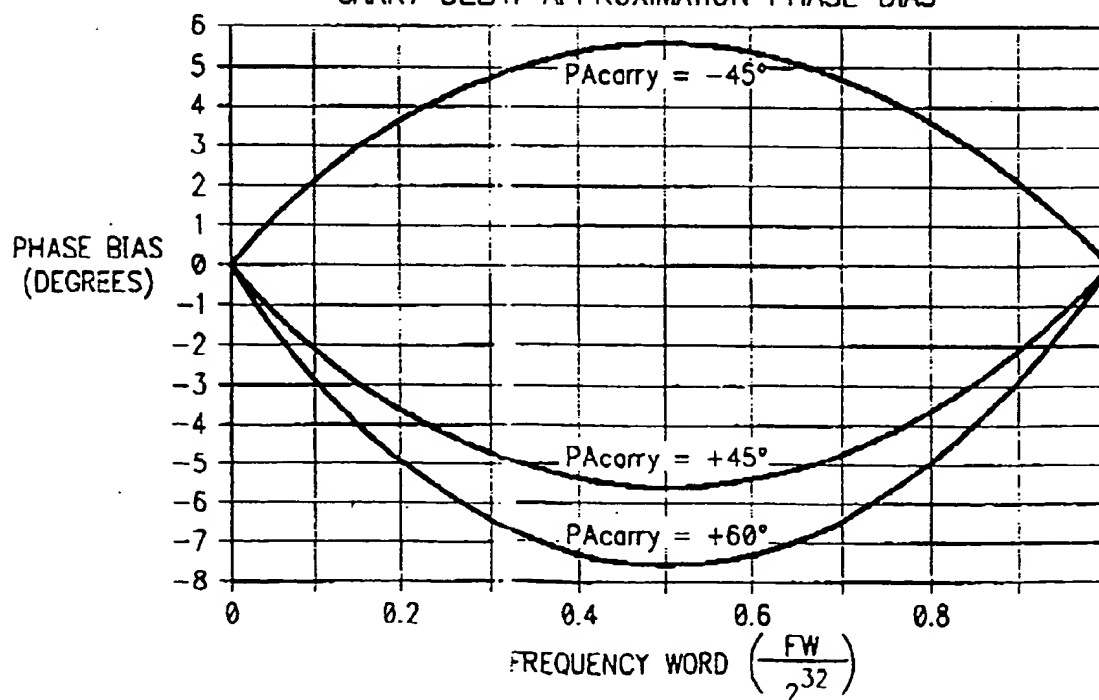
FIG. 14
PHASE SETTABILITY AS A FUNCTION OF d

d	PHASE SETTABILITY	
	40.92 MHz (NS=8)	57.792 MHz (NS=6)
1	45.0	60.0
2	22.5	30.0
3	15.0	20.0
4	11.3	15.0
5	9.0	12.0
6	7.5	10.0
7	6.4	8.6
8	5.6	7.5
9	5.0	6.7
10	4.5	6.0
11	4.1	5.5
12	3.6	5.0
13	3.5	4.6
14	3.2	4.3
15	3.0	4.0
16	2.8	3.8
17	2.7	3.6
18	2.5	3.3
19	2.4	3.2
20	2.3	3.0
21	2.2	2.9
22	2.1	2.8
23	2.0	2.7
24	< 2.0	2.5
25	<< 2.0	2.4
26	<<< 2.0	2.4
27	<<< 2.0	2.3
28	<< 2.0	2.2
29	< 2.0	2.1
30	< 2.0	2.0

FIG. 19
PHASE RANGE OF EACH STATE
IN THE 40.92 AND 40.9216 MHz PLANS

+112.5°   110 (S=2) 1   +67.5°

111 (S=3) 1   101 (S=1) 1

+157.5°   +22.5°

000 (S=4) 0   100 (S=0) 1

001 (S=5) 0   011 (S=7) 0   +22.5°

+202.5°   010 (S=6) 0   -22.5°

+247.5°   +292.5°
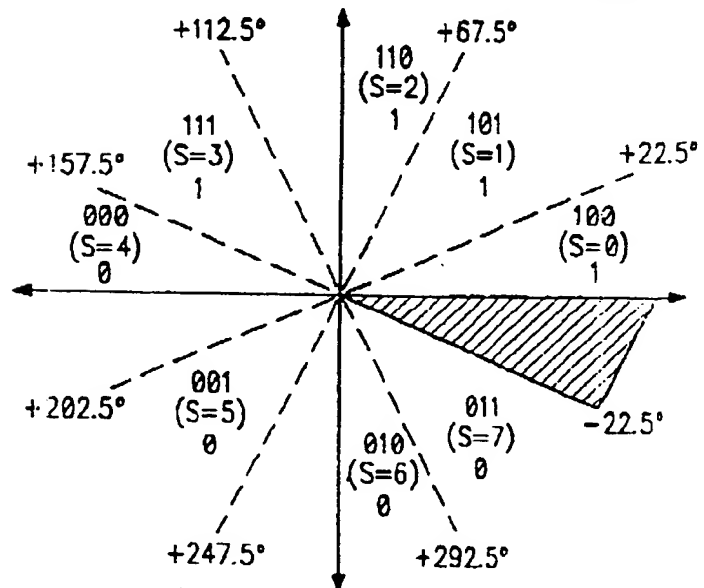
▨ REGION WHERE X1 MUST BE INCREMENTED BY 1
BECAUSE FIRST RISING EDGE OF A NEW SET-UP
DOES NOT OCCUR.

FIG. 15

57,792 PHASE ANOMALIES
(FOR DOPPLER -11,000 TO +11,000 M/S)

NORMAL CODE CLOCK
FREQUENCY WORD RANGE
NO PHASE ANOMALIES

PHASE SETTABILITY
(DEGREES)

FREQUENCY WORD $\left(\dfrac{FW}{2^{32}}\right)$

23

FIG. 16

40.9216 PHASE ANOMALIES
(FOR DOPPLER -11,000 TO +11,000 M/S)

45.0° PHASE ANOMALY AT
A DOPPLER OF +11,428 M/S

PHASE SETTABILITY
(DEGREES)

FREQUENCY WORD $\left(\dfrac{FW}{2^{32}}\right)$
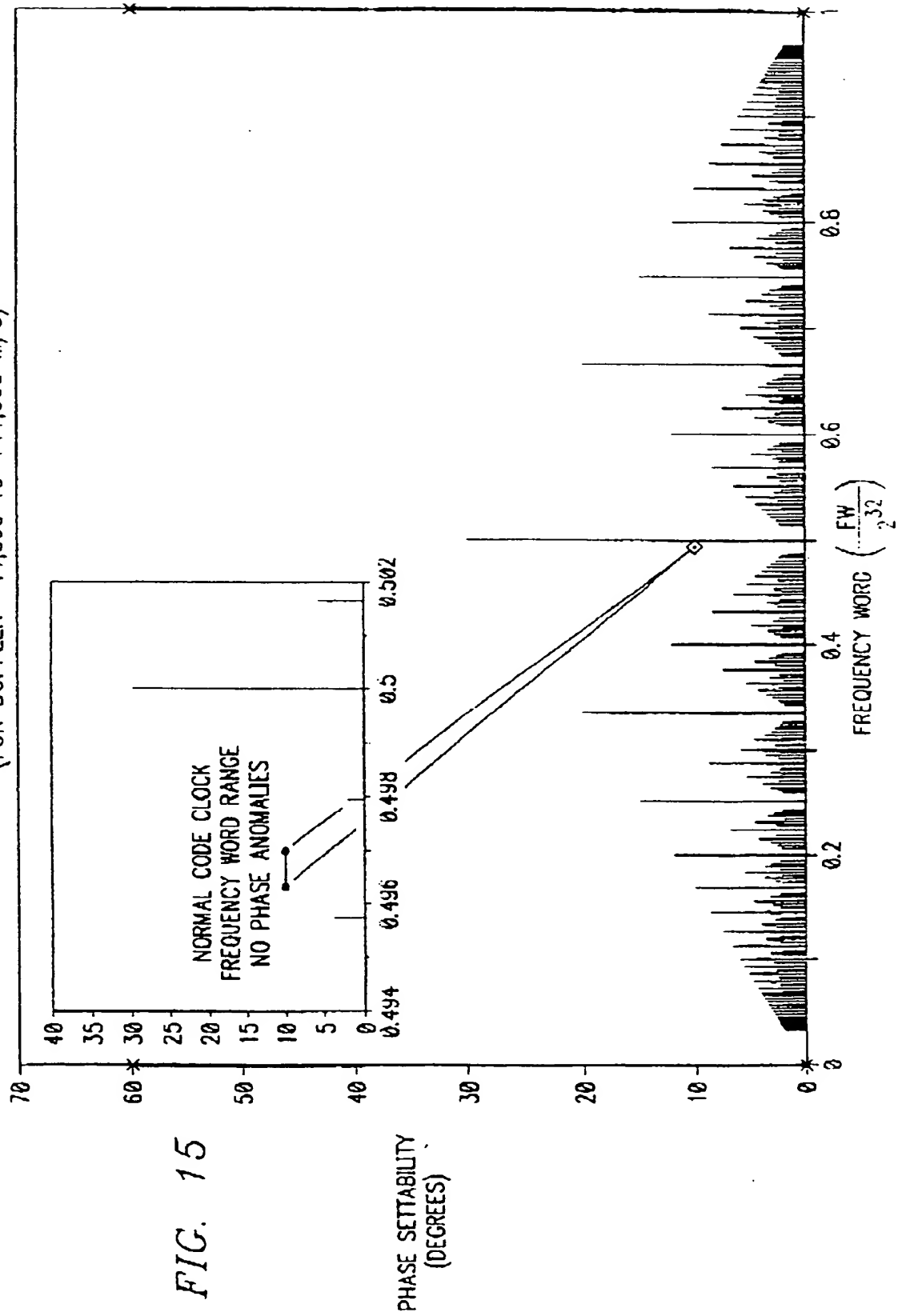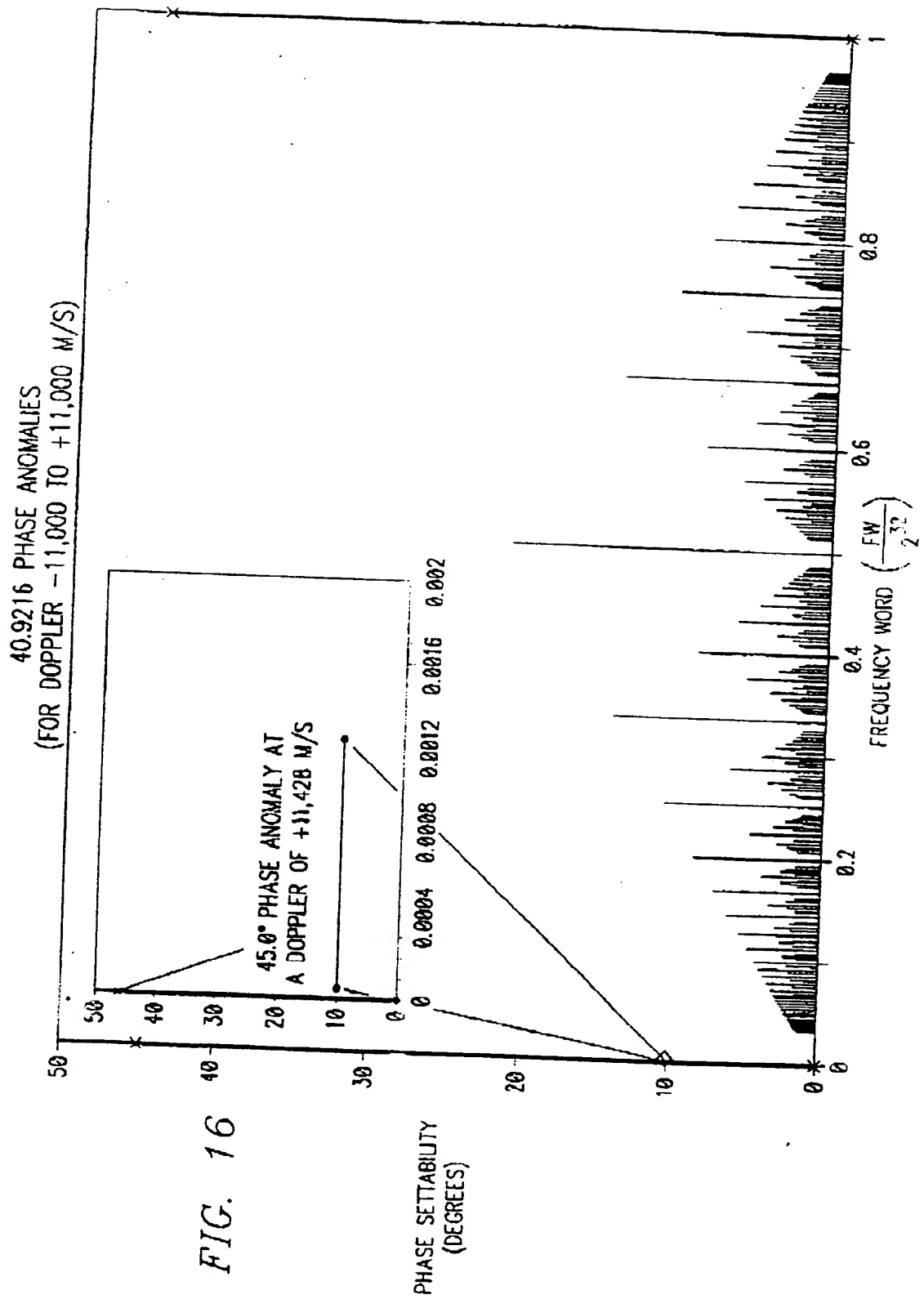
FIG. 17

40.9200 PHASE ANOMALIES
(FOR DOPPLER −11,000 TO +11,000 M/S)

PHASE SETTABILITY
(DEGREES)

45.0° PHASE ANOMALY AT CENTER FREQUENCY

FREQUENCY WORD $\left(\dfrac{FW}{2^{32}}\right)$

FIG. 20
PHASE RANGE OF EACH STATE
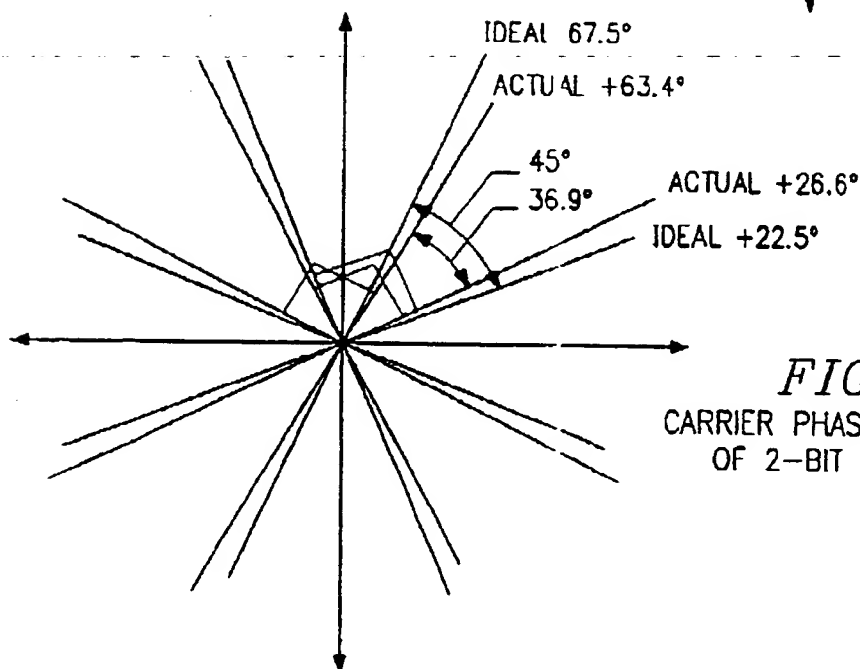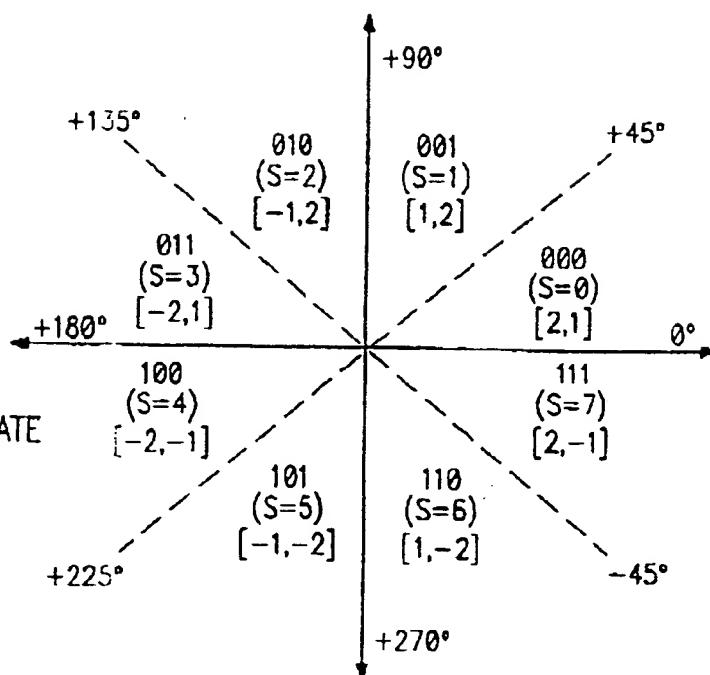
FIG. 21
CARRIER PHASE BIAS BECAUSE
OF 2-BIT QUANTIZATION

FIG. 23
(PRIOR ART)

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FIG. 22

CARRIER PHASE ANOMALIES
(FOR DOPPLER -11,000 TO +11,000 M/S)

49.1° PHASE ANOMALY
AT CENTER FREQUENCY
FOR BOTH L1 AND L2

53.1° PHASE ANOMALY AT
A DOPPLER OF +11,733 M/S
FOR BOTH L1 AND L2

7.5° PHASE ANOMALY AT A
DOPPLER OF -8,565 M/S

22.5° PHASE ANOMALY AT
A DOPPLER OF +6,967 M/S

7.6° PHASE ANOMALY AT
A DOPPLER OF -8,800 M/S

9.0° PHASE ANOMALY AT
A DOPPLER OF -8,800 M/S

17.7° PHASE ANOMALY AT
A DOPPLER OF +2,667 M/S

PHASE SETTABILITY
(DEGREES)

FREQUENCY WORD $\left(\dfrac{FW}{2^{32}}\right)$

A — L1, 40.9200 MHz
B — L2, 40.9200 MHz
C — L1, 40.9216 MHz
C — L2, 40.9216 MHz
E — L1, 57.792 MHz
F — L2, 57.792 MHz

FIG. 24

FIG 25

FIG 26

6-BIT RIPPLE COUNTER WITH TRANSMISSION GATE PULSE INJECTORS
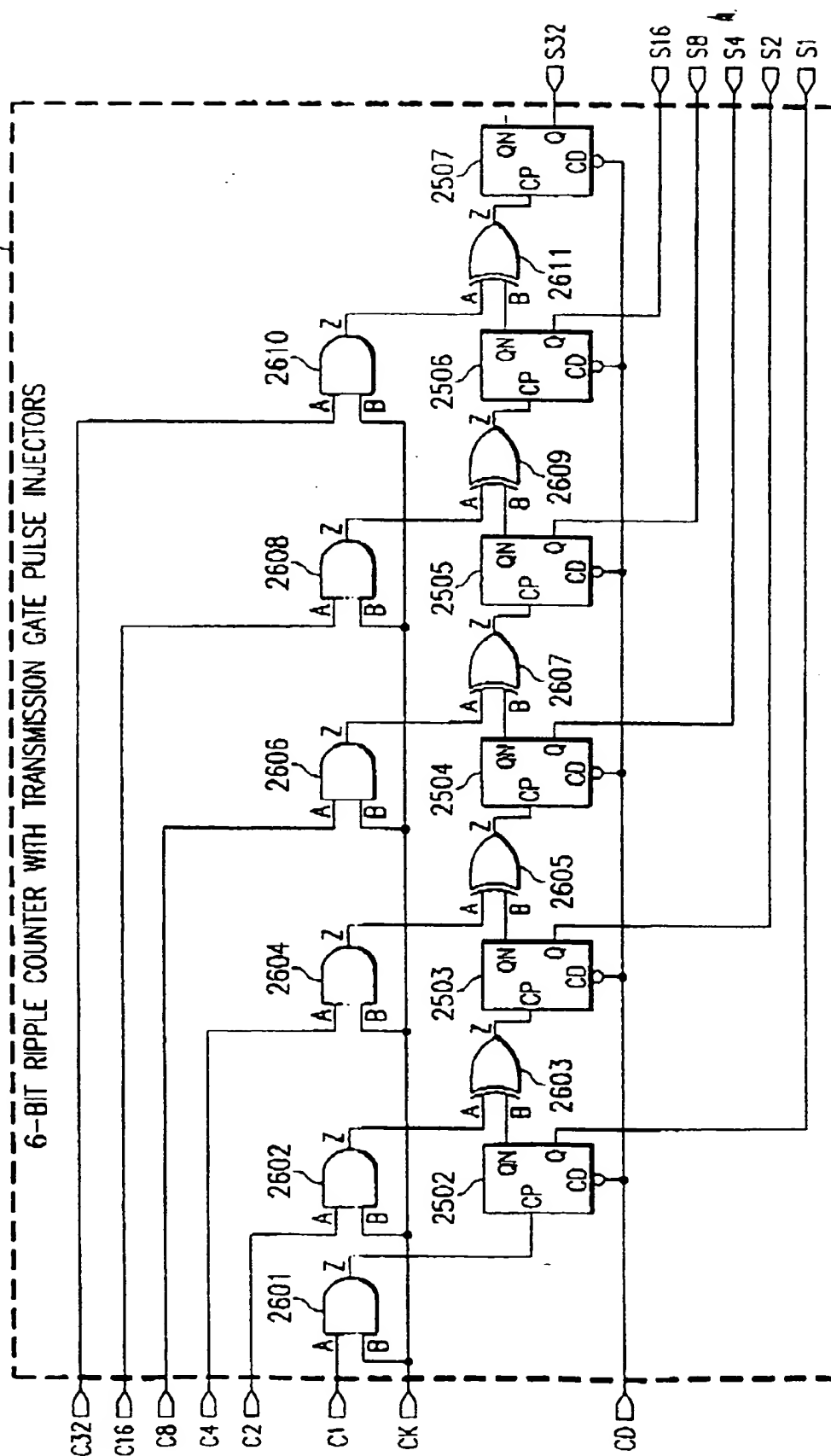
FIG. 27

6-BIT RIPPLE COUNTER WITH BOOLEAN PULSE INJECTORS

FIG. 28

FIG. 29
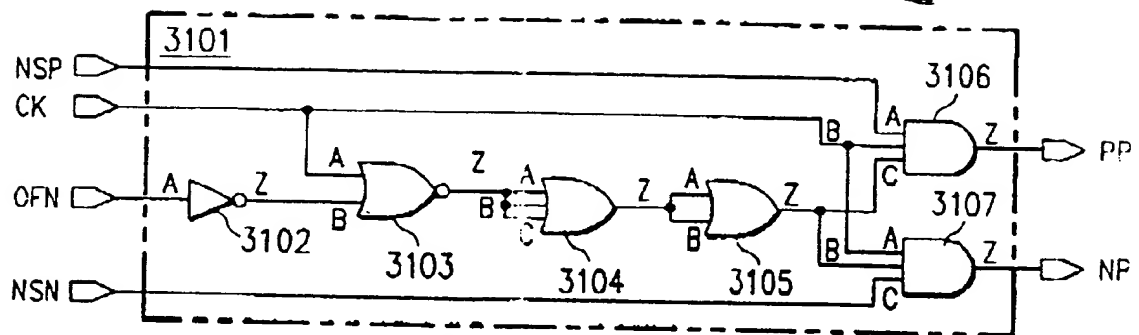### INTERMEDIATE CORRELATOR MODULE BLOCK DIAGRAM

FIG. 30

FIG. 31
PULSE GENERATOR

CK – THE REFERENCE CLOCK
OFN – OFF, ASSERTED LOW
NSP – NOISE SIGN POSITIVE, ASSERTED HIGH
NSN – NOISE SIGN NEGATIVE, ASSERTED HIGH
PP – PULSE FOR POSITIVE VALUE ACCUMULATOR
NP – PULSE FOR NEGATIVE VALUE ACCUMULATOR

DECIMAL	SIGN	MAGNITUDE
−32	1	100000
−16	1	010000
−8	1	001000
−4	1	000100
−2	1	000010
−1	1	000001
0	0 or 1	000000
+1	0	000001
+2	0	000010
+4	0	000100
+8	0	001000
+16	0	010000
+32	0	100000

FIG. 32
VALID INPUTS FOR
NORMAL OPERATION OF
ADDER/ACCUMULATOR

FIG. 35
NON–BINARY MULTIPLE
MAGNITUDE VALUES
WHICH MAY PRODUCE
DETERMINATE RESULTS IN
ADDER/ACCUMULATOR
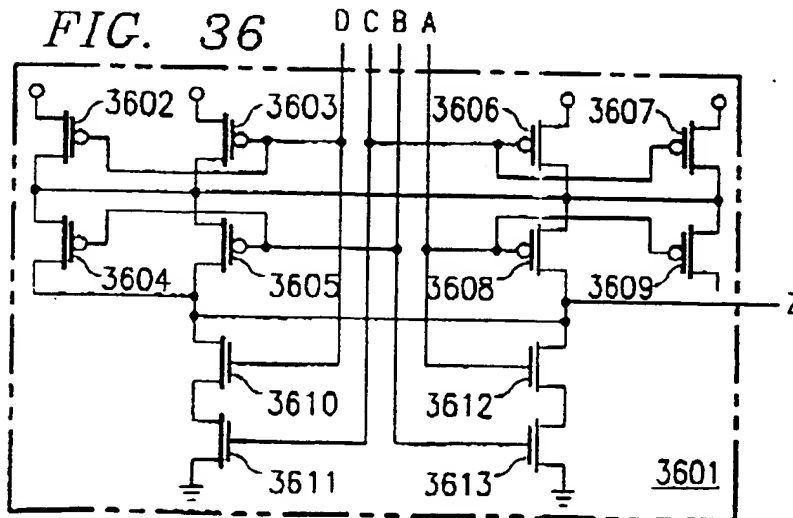
000101	5
001001	9
001010	10
010001	17
010010	18
010100	20
010101	21
100001	33
100010	34
100100	36
100101	37
101000	40
101001	41
101010	42

FIG. 36

FIG. 33

AN EXAMPLE OF OPERATION OF PAIRED ADDER/ACCUMULATORS

STEP	INPUT FROM THE FRONT-END CORRELATOR MODULE 201		POSITIVE VALUE INTEGRATION		NEGATIVE VALUE INTEGRATION		CARRIES TO THE BACK-END CORRELATOR MODULE 203
START			000000	(0)	000000	(0)	
1	1 100000	(−32)	000000	(0)	100000	(32)	NONE
2	0 000100	(+4)	000100	(4)	100000	(32)	NONE
3	1 010000	(−16)	000100	(4)	110000	(48)	NONE
4	1 000010	(−2)	000100	(4)	110010	(50)	NONE
5	0 010000	(+16)	010100	(20)	110010	(50)	NONE
6	1 010000	(−16)	010100	(20)	000010	(2)	NEGATIVE
7	0 000010	(+2)	010110	(22)	000010	(2)	NONE
8	0 000001	(+1)	010111	(23)	000010	(2)	NONE
9	1 100000	(−32)	010111	(23)	100010	(34)	NONE
10	1 000100	(−8)	010111	(23)	100110	(42)	NONE
11	0 100000	(+32)	110111	(55)	100110	(42)	NONE
12	1 000010	(−2)	110111	(55)	101000	(44)	NONE
13	0 001000	(+8)	111111	(63)	101000	(44)	NONE
14	1 100000	(−32)	111111	(63)	001000	(8)	NEGATIVE
15	0 000001	(+1)	000000	(0)	001000	(8)	POSITIVE

FIG. 34

MAGNITUDE VALUES WHICH ALWAYS CAUSE INDETERMINATE RESULTS IN ADDER/ACCUMULATORS

000011	3	011100	28	110011	51
000110	6	011101	29	110100	52
000111	7	011110	30	110101	53
001011	11	011111	31	110110	54
001100	12	100011	35	110111	55
001101	13	100110	38	111000	56
001110	14	100111	39	111001	57
001111	15	101011	43	111010	58
010011	19	101100	44	111011	59
010110	22	101101	45	111100	60
010111	23	101110	46	111101	61
011000	24	101111	47	111110	62
011001	25	110000	48	111111	63
011010	26	110001	49		
011011	27	110010	50		

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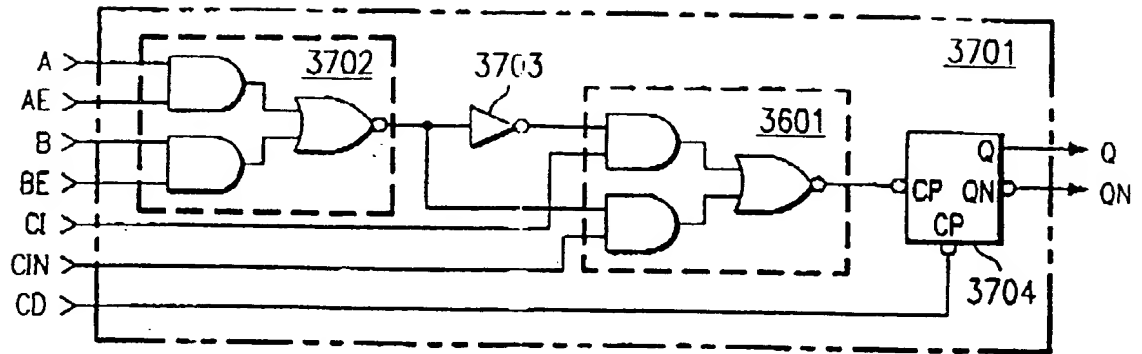
FIG. 37

FIG. 44

ADJACENT CORRELATOR PRESUMMING

NOTE Z_7 IS NOT A SUM

NOTE: WHEN PRESUMMING IS OFF $Z_i = I_i + jQ_i$
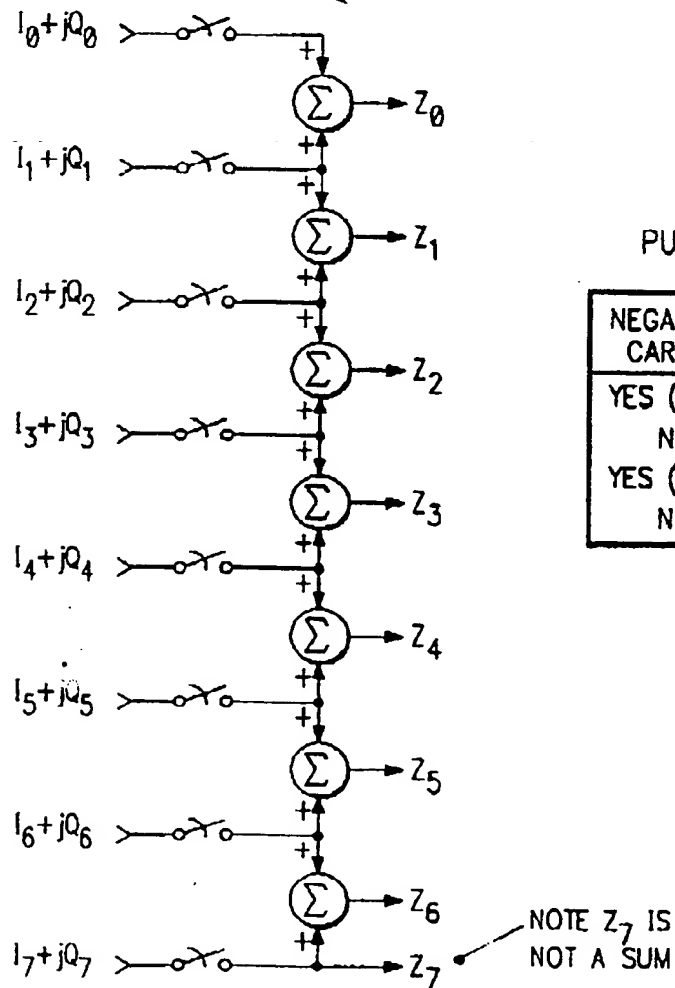
FIG. 42

PULSE ENCODER OPERATION

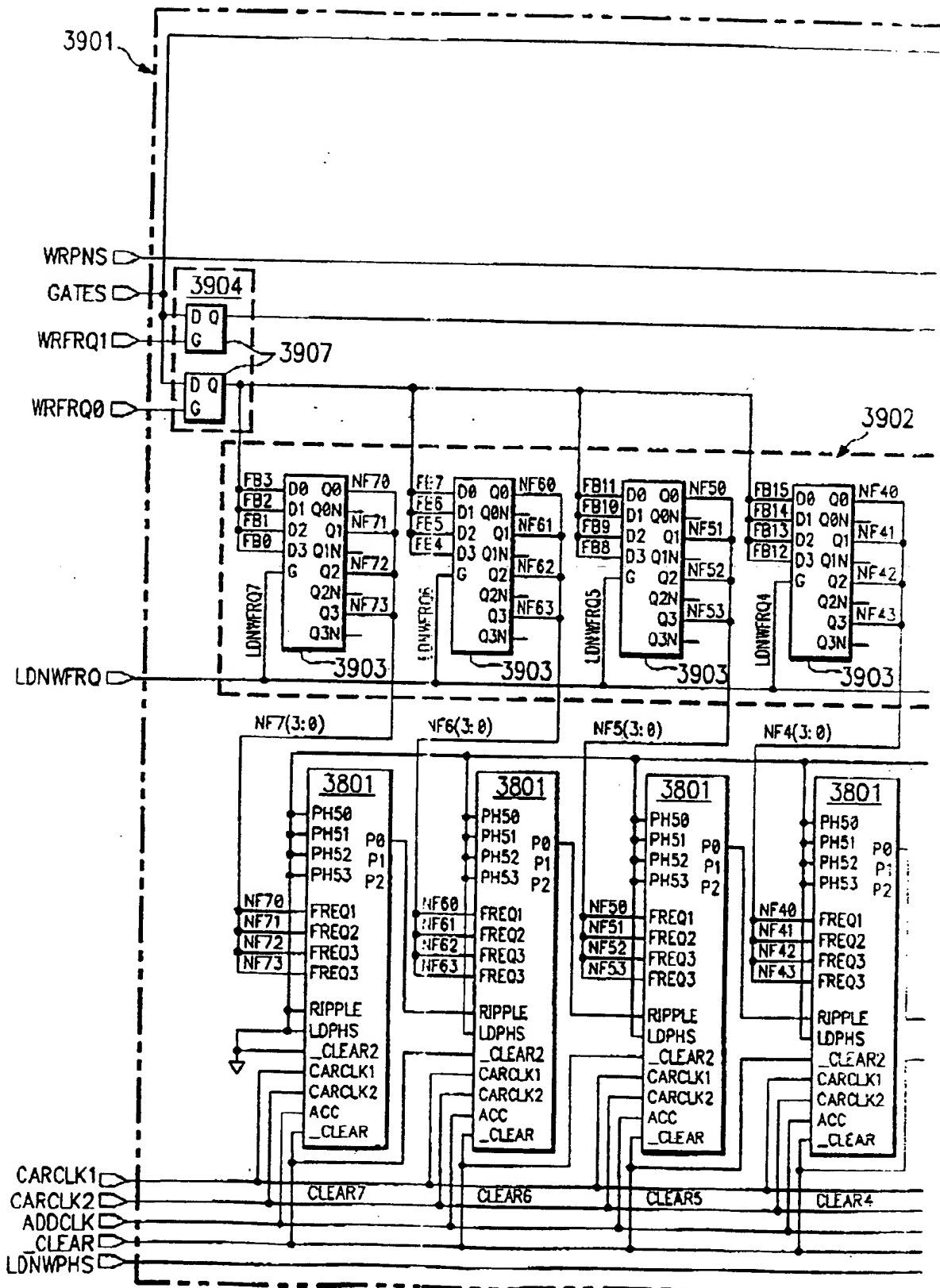| NEGATIVE CARRY	POSITIVE CARRY	BIAS	OUTPUT PULSE
YES (−1)	NO	+1	NONE (0)
NO	NO	+1	+1
YES (−1)	YES (+1)	+1	+1
NO	YES (+1)	+1	+2

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FIG. 38

4-BIT ADDER/ACCUMULATOR WITH CARRY

FIG. 39a

FIG. 39b

FIG. 40

FIG. 41

FIG. 43
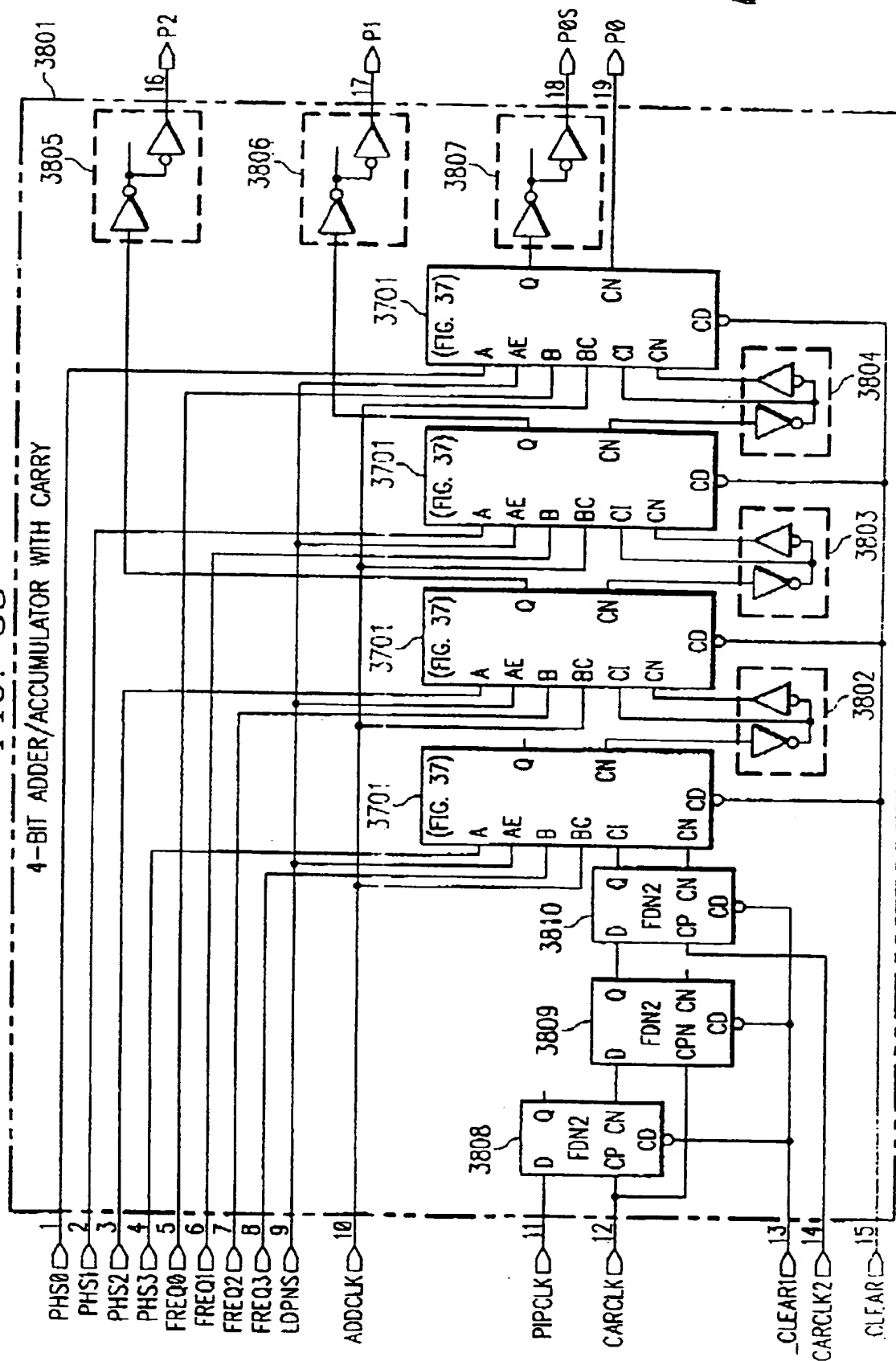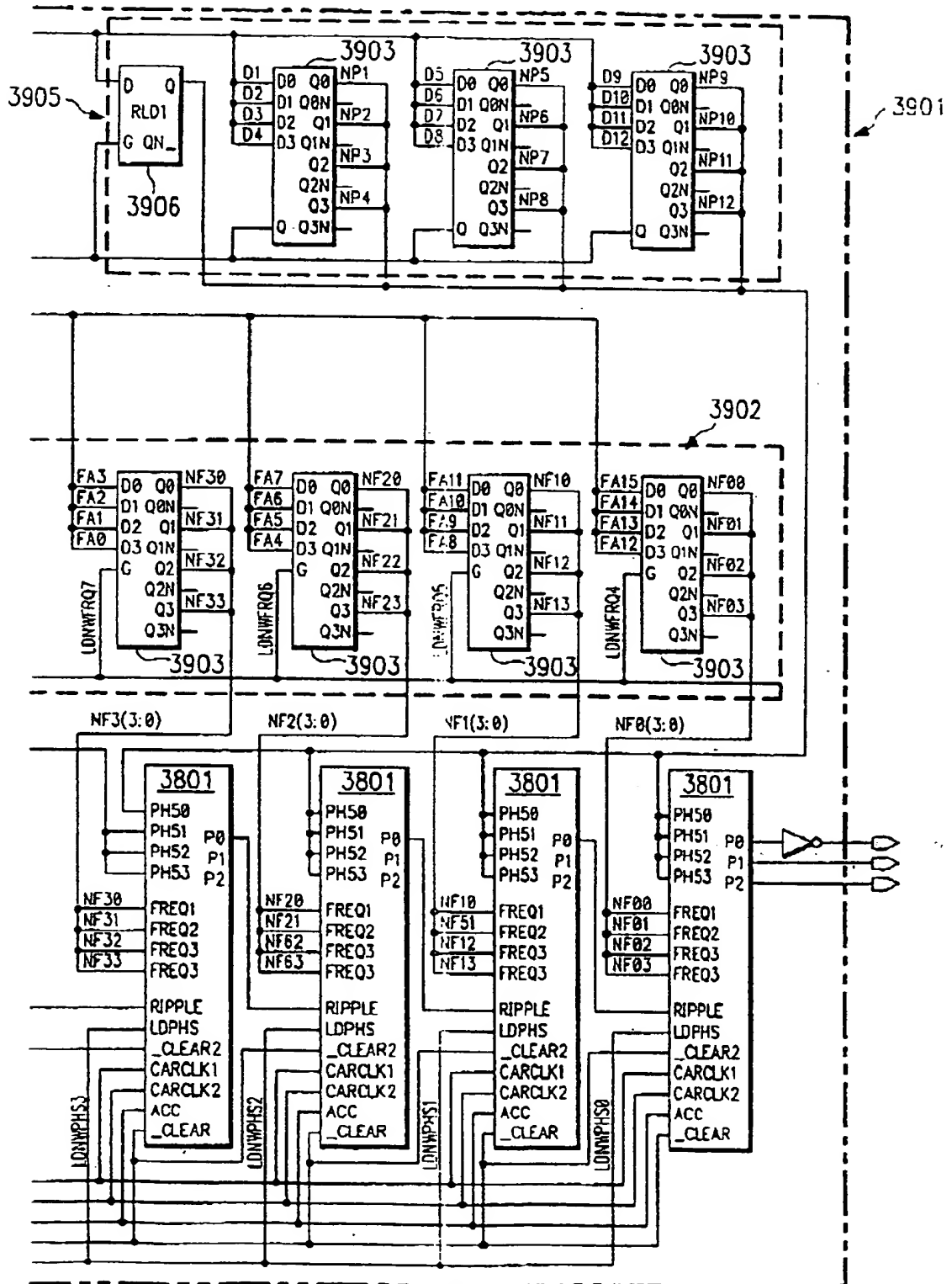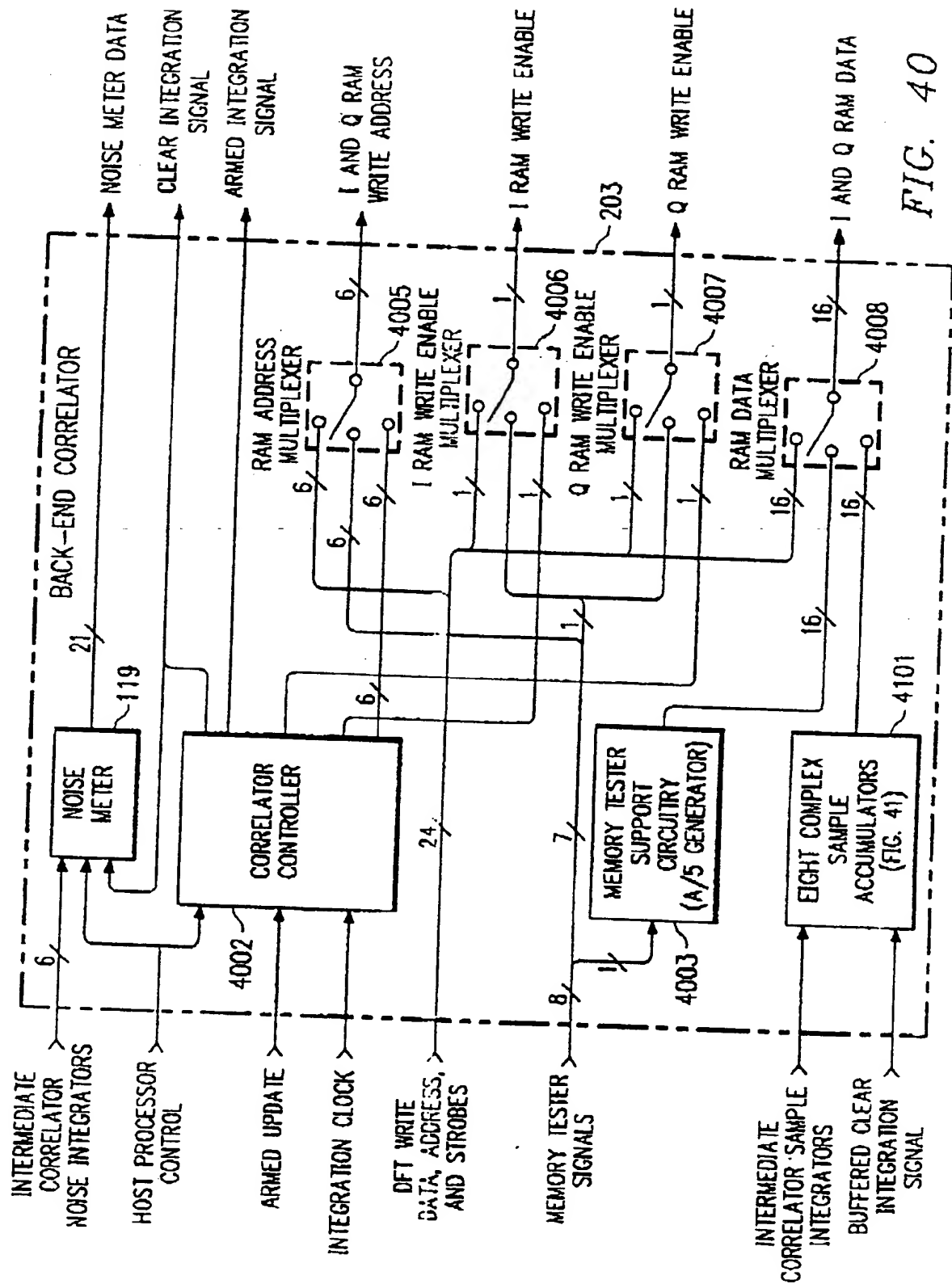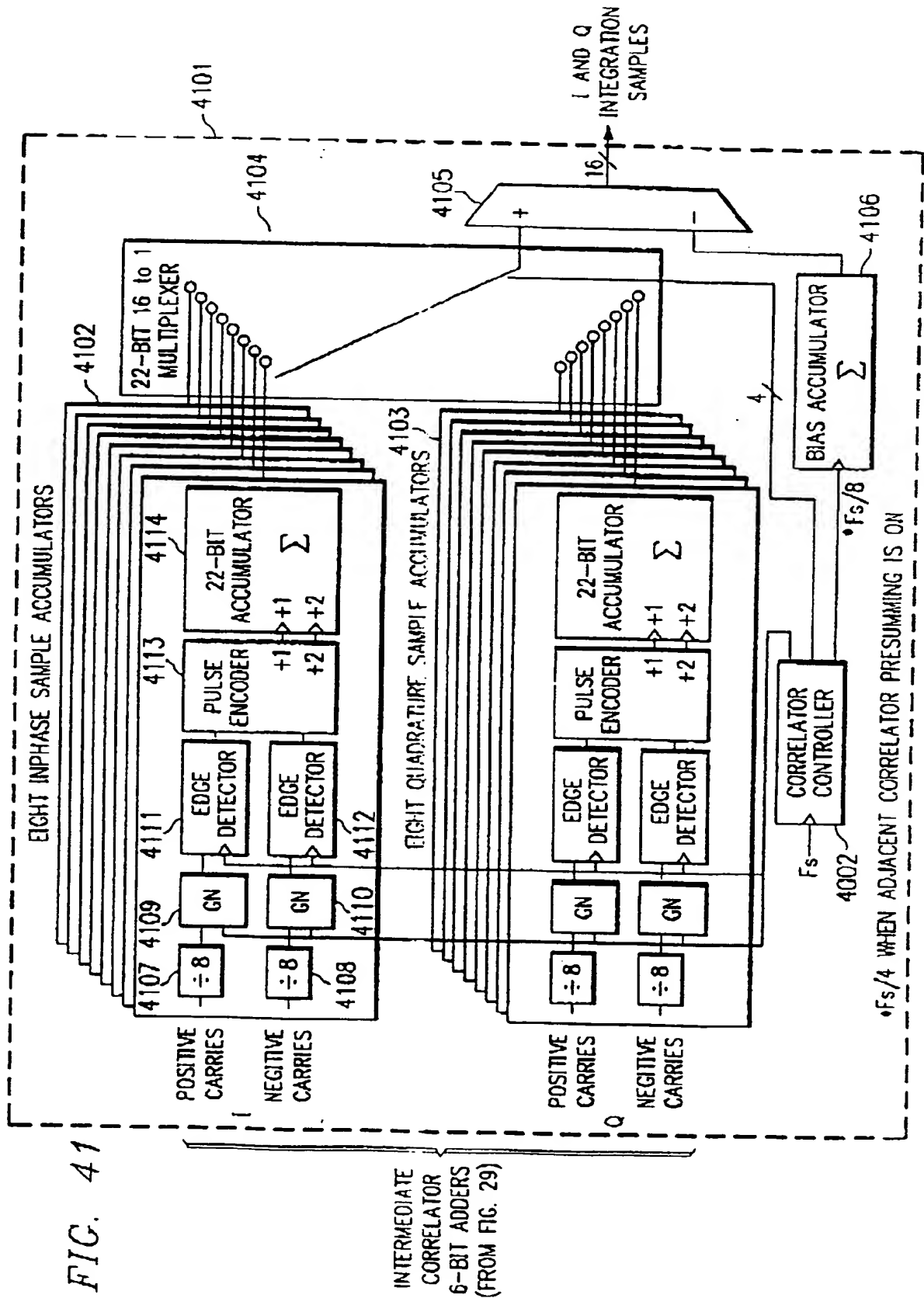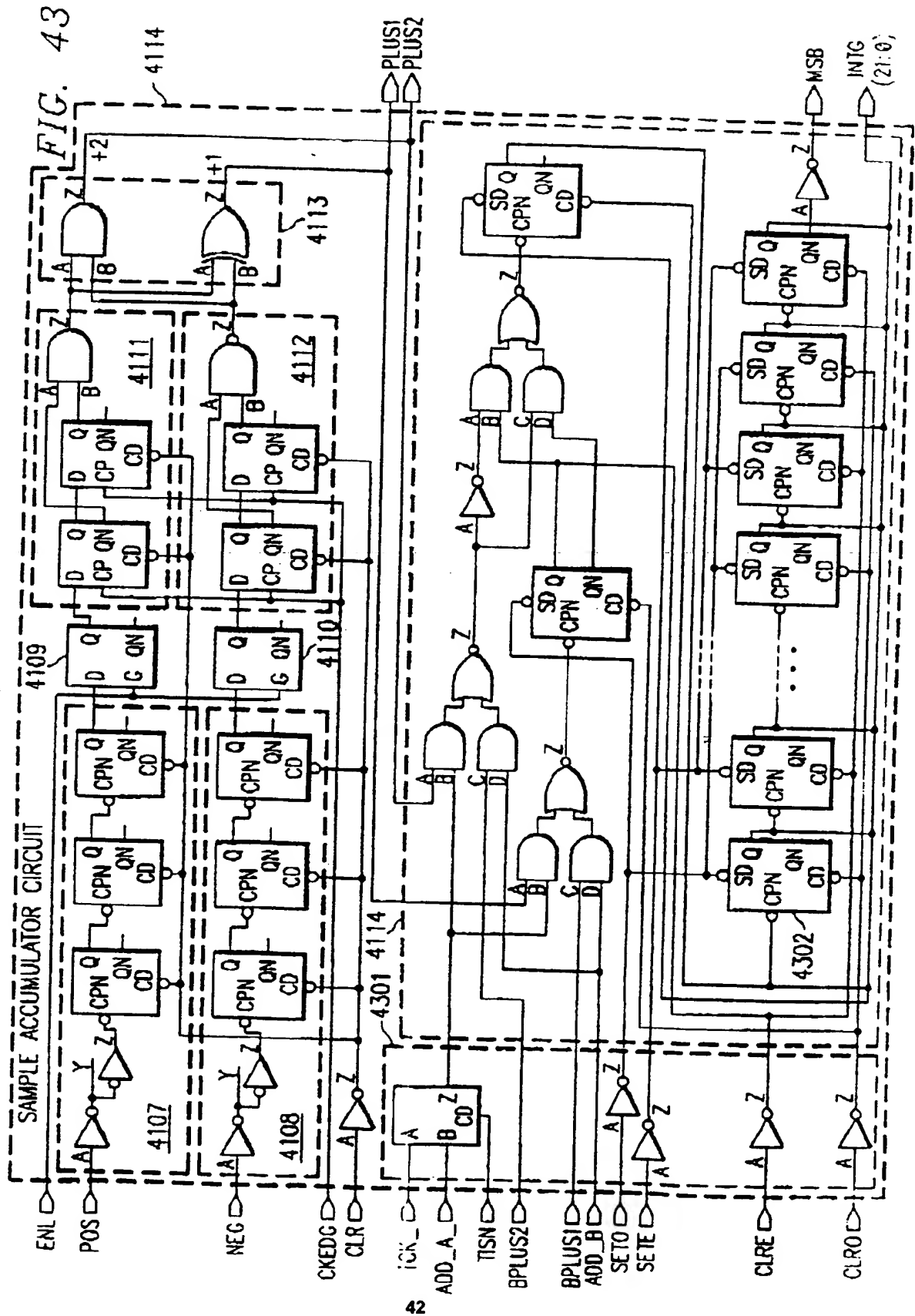
FIG. 45
RELATIVE SNR WITH PRE−SUMMING OFF

$\eta = -1.13dB$

−2.5 dB

CODE ERROR (CHIPS)
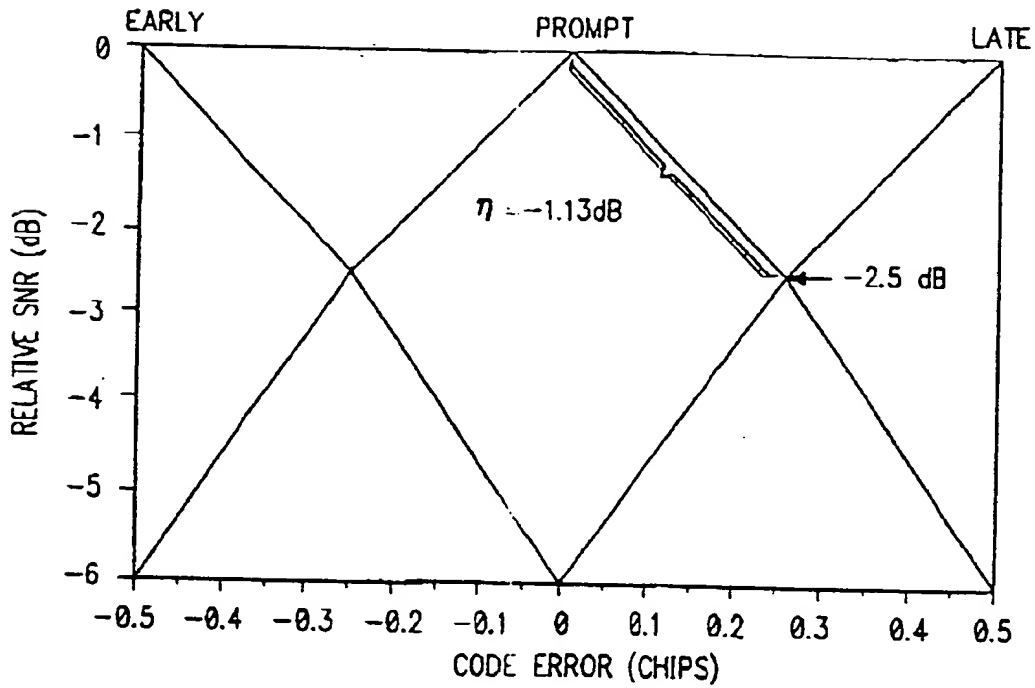
FIG. 46
RELATIVE SNR WITH PRE−SUMMING ON

EARLY   PROMPT   LATE   −1.25 dB

CODE ERROR (CHIPS)

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EP 0 501 828 A1
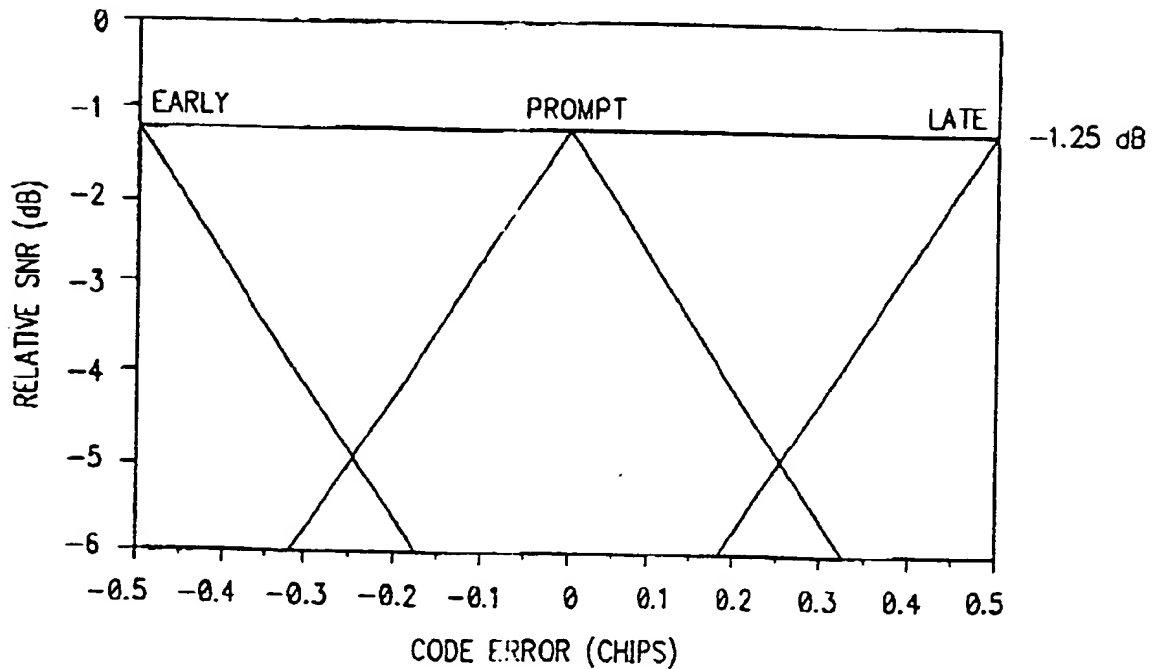
European Patent Office

EUROPEAN SEARCH REPORT

Application Number

	DOCUMENTS CONSIDERED TO BE RELEVANT		EP 92301740.4
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP - A - 0 351 156 (ASHTECH) * Abstract; fig. 1; claims 1,4,11,12 *	1,10	G 01 S 5/14
A	GB - A - 2 153 177 (STANDARD TELEPHONES) * Abstract; claims 1,7 *	1,10	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G 01 S

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	05-06-1992	FUSSY

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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L : document cited for other reasons

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